DESIGN OF ENERGY EFFICIENT FPGA ARCHITECTURE FOR MODERATE SPEED APPLICATIONS

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Submitted By

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CERTIFICATE

This is to certify that the thesis entitled **"Design of Energy Efficient FPGA Architecture for Moderate Speed Applications"**, submitted by **Mr. Satish Mohanrao Turkane** in partial fulfillment of requirement for the award of the degree of Doctor of Philosophy in Electronics & Telecommunication Engineering at Matoshri College of Engineering and Research Center, Nashik of Savitribai Phule Pune University, Pune is a bonafide record of the research work carried out by him. He had worked under the supervision of **Dr. Abdul Kadir Kureshi**. He has fulfilled the requirement of the submission of the thesis. The material obtained from other sources has been duly acknowledged in the thesis. The results embodied in this thesis have not been submitted to any other institute or university for the award of any degree or diploma.

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Certified that this work entitled **"Design of Energy Efficient FPGA Architecture for Moderate Speed Applications",** is being submitted by **Mr. Satish Mohanrao Turkane,** in partial fulfillment of the requirements for the award of the degree of Doctor of Philosophy in Electronics & Telecommunication Engineering from Savitribai Phule Pune University, Pune, India.

This is a record of candidate's own work under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

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DECLARATION

This is to declare that the thesis entitled **"Design of Energy Efficient FPGA Architecture for Moderate Speed Applications",** submitted by me for the award of degree of Doctor of Philosophy in Electronics & Telecommunication Engineering; is the record of work carried out by me at Matoshri College of Engineering and Research Center, Eklahare, Nashik.

The said work is carried out during the period 02/08/2014 to 26/02/2018 under the guidance of **Dr. A. K. Kureshi** and has not formed the basis for the award of any degree, diploma, associate ship, fellowship, titles in this or any other university or other institution of higher learning.

I further declare that the material obtained from other sources has been duly acknowledged in the thesis.

Satish M. Turkane

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CONTENTS

ABSTRACT

There are two sources of energy utilization in CMOS in particular dynamic and leakage. The dynamic power in CMOS is a quadratic capacity of the supply voltage and the leakage control is its exponential capacity. Henceforth, the best approach to decrease the power utilization is through supply voltage scaling. The outrageous instance of supply voltage scaling is the subthreshold administration which is scaled beneath the limit voltage to accomplish ultra-low power. The leakage current is utilized as a driving current in subthreshold circuits and consequently, the speed degrades impressively. In spite of the speed degradation, very few researchers have attempted to enhance the speed under subthreshold conditions.

This postulation presents innovative techniques to enhance the speed and energy of subthreshold circuits with an obliged control spending intends to amplify their application territory. There is an immense market for ultra-low power applications which is being ruled by ASIC. Consequently, it is fundamental to expand the range of FPGA even under subthreshold conditions with the objective that they can similarly be used for reconfigurable ultra-low power applications set up of the exorbitant and more unyielding ASICs in future developments. This postulation proposes the Post-CMOS device of Tunnel Filed Effect Transistor which is having significant advantage as compared to conventional CMOS device. Finally, device parameters like channel length, substrate and halo doping concentrations, and oxide thickness of Si-MOSFET being optimized using TCAD tools for better circuit performance at deep nanometer technology node. This device will have significantly enhanced speed, lowered the delay and power.

The FPGA interconnect assets execution has been improved utilizing gadget enhancement procedures under subthreshold conditions. Interconnect fundaments decides the execution of frameworks at the Nano scale. Henceforth, the outline of interconnect is must in enhancing the execution under subthreshold conditions. Simulation work is executed on the emerging Interconnect viz. CNT, GNR etc. and reported significant improvements in terms of area, power and delay.

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LIST OF SYMBOLS

Symbols	Description
ϕox	Barrier height for the tunneling particles
γ	Body effect coefficient
V_{bs}	Body-to-Source Voltage
kB	Boltzmann's constant
$C_{g,Avg}$	Average Capacitance across the gate bias
C_{dm}	Capacitance of depletion layer
C_c	Coupling Capacitance
L	Channel length
n, m	Chiral vector
F_{cen}	Centre oscillating frequency of VCO
F	Clock frequency
θ	Chirality angle
A	Device cross sectional area
h	Distance between the gate and the CNT centre
V_{ds}	Drain-to-Source Voltage
P_{dy}	Dynamic power dissipation
q	Elementary charge
m	Electron powerful mass
fs	Fermi distribution in source
fd	Fermi distribution in drain
Hox	Gate dielectric thickness between the CNT centre and gate
Cox	Gate oxide capacitance
Tox	Gate oxide thickness
K	Gate oxide material
V_{gs}	Gate-to-Source Voltage
φ_m	Gate work-function
T_{int}	Interconnect delay
a	Lattice constant
C_L	Loading capacitance
$T_{logicmax}$	Maximum logic gate delay

Symbols	Description
N_{ch}	Number of conducting channels
A and B	Physical parameters.
$\hbar$	Planck's constant
V_{ox}	Potential drop across the thin oxide layer
V_G	Potential of transistor's gate
V_{DD}	Power Supply Voltage
ρm	Probability of metallic CNT
Ps	Source resistance per unit length of doped CNT
ϕF	Substrate Fermi potential
n	Subthreshold swing coefficient
V	Supply Voltage
α	Switching factor (or activity factor)
g_m	Transconductance
T_{C_Q}	Time between the initial register after the clock signal arrives
T_{setup}	Time required of the receiving register
Vth	Threshold voltage
V_T	Thermal voltage
W/L	Width/Length of transistor
φs	Work function
μo	Zero bias mobility

LIST OF ABBREVIATIONS

Symbols	Description
Al	Aluminum
ASIC	Application Specific Integrated Circuits
BTBT	Band-to-Band Tunneling
BLE	Basic Logic Element
CNT	Carbon Nano-tube
CNFET	Carbon Nanotube Field Effect Transistor
CNIA	Carbon Nanotube Interconnect Analyser
CLBs	Configurable Logic Blocks
CPLDs	Complex Programmable Logic Devices
CAD	Computer Aided Design
Cu	Copper
DIL	Driver Interconnect Load
DIBN	Drain Induced Barrier Narrowing
I_{EDT}	Edge Direct Tunnelling Current
FBB	Forward Body Bias
FPGA	Field Programmable Gate Array
FinFET	Fin Field Effect Transistor
GIDL	Gate-Induced Drain Leakage
GNR	Graphene Nano ribbon
Au	Gold
LUT	Look Up Table
MLGNR	Multi-Layer Graphene Nano ribbon
MOSFET	Metal oxide semiconductor field effect transistor
MCB	Mixed Carbon Bundle
MWCNT	Multi Walled Carbon Nanotube
MTCMOS	Multi-Threshold CMOS
NTRS	National Technology Roadmap for Semiconductors
I_{ON}	On Current
I_{OFF}	OFF Current
IEA	International Energy Agency
ITRS	International Technology Roadmap of Semiconductors

Symbols	Description
IC	Integrated Circuit
PLL	Phase Lock Loop
PDP	Power delay product
Pd	Power dissipation
PVT	Process-Voltage-Temperature
PROM	Programmable Read-Only Memory
PAL	Programmable Array Logic
PLA	Programmable Logic Array
PD	Propagation Delay
RC	Resistance-Capacitance
RRAM	Resistive Random Access Memory
RBB	Reverse Body Bias
SCE	Short Channel Effect
SiO_2	Silicon Dioxide
SPLDs	Simple Programmable Logic Devices
SLGNR	Single Layer Graphene Nano ribbon
SWCNT	Single Walled Carbon Nanotube
SCVCO	Source Coupled Voltage Controlled Oscillator
SSASPL	Static differential Sense Amplifier based Shared Pulsed Latch
SS	Subthreshold Swing
STT	Surface Tunnel Transistor
I_{leak}	Switch off leakage current of MOSFET
TFET	Tunnel Field Effect Transistors
ULP	Ultra-low power

Chapter 1

INTRODUCTION

1.1 Field Programmable Gate Arrays

Field Programmable Gate Array (FPGA) is a pre-produced silicon device that can be organized to wind up detectably any kind of automated circuits or structures. The “reconfigurable”, term in FPGA exhibits an ability to change its helpfulness even after creation. FPGAs are mainstream decisions for advanced circuit usage as a result of their developing thickness, speed, short outline cycle, and relentlessly diminishing expense. However the control utilization, particularly leakage control, has turned into a noteworthy outline leap for the semiconductor business at the nanoscale administration. The versatility and the adaptability of FPGA lies in its reconfigurability. On the contrary it comes at the cost of additional hardware coming about more power scattering and longer postponement. However, Application specific integrated circuits (ASIC) are more power productive than FPGA yet they are expensive to bring down volume and more hard to plan at a nanoscale. To produce a useful ASIC it attracts various key issues as mentioned belows [1]:

- Deep submicron ASIC Computer Aided Design (CAD) apparatuses for combination; position, directing, extraction, reenactment timing, and power examination so expensive.
- The cost of a mask of a totally made device is in a colossal number of dollars. This cost can be diminished if prototyping costs are shared among different smaller ASICs.
- The high production cost to develop a ASIC.

Likewise, if concentrated on nature of ASIC makes it hard to reuse it for different advantageous applications. Moreover, higher cost and need for a generally higher rate of benefit asks most mechanized structure affirmation in FPGA notwithstanding its higher power usage. The accompanying essential focal points of FPGAs pull in analysts and produces to every now and then redesign the FPGA innovation.

- Minimum time to advertise when contrasted with ASICs.
- FPGAs are magnificent possibility for low volume generation.

- FPGAs are perfect for prototyping purposes. Equipment testing and check can be immediately performed on the chip.

Eventually the execution of reconfigurable structures has been rapidly upgrading to associate the execution opening with ASICs. Past research work was based on subthreshold method of reasoning arrangement to enhance the life of the battery of predominantly application specific reduced devices [2-6]. Along with these lines, it is moreover indispensable to look at the probability of widening the use of FPGA even in subthreshold region, with the objective that minimized essential profitable systems can utilize the reconfigurability feature of FPGA [7].

Regardless, FPGA requires 20 to 35X more region than a standard cell ASIC and speed execution roughly 3 to 4X slower than ASIC and moreover requires around 10X higher dynamic power [8]. Thus, it is basic to look at particular systems for diminishing the power use in FPGA, with the objective that it can moreover be used set up of ASICs even in essentialness obliged applications. It has been settled that interconnect resources of FPGA use most of the chip power, region, and chooses the general circuit delay [7, 9]. In spite of the fact that subthreshold operation of FPGA lessens control dispersal by a request of extent however it brings about noteworthy defer overhead. Improving the speed of subthreshold FPGA is an imperative arrangement challenge at the circuit and device levels to stretch out their application region to ultra-low power (ULP) remote sensor frameworks and biomedical applications.

1.2 Motivation

CMOS technology scaling helps in achieving the desired speed yet at the cost of extended power spread [10-12]. Regardless, there is a remarkable class of creating ULP applications like body sensor frameworks, RFIDs, pacemaker, etc. does not require fast speed. The fundamental motivation for these applications is ULP use so as to drag out the battery life or to use essential gathering suitably [13-14]. To satisfy the ULP for these applications, it is vital to work the circuit under subthreshold condition [13]. FPGAs are ultimate choice for computerized framework usage due to their developing thickness, speed, short outline cycle, and consistently diminishing expenses. The power advancement has pulled in expanded consideration because of the quick development of individual remote correspondence, battery fueled devices and compact computerized applications. In addition, a large percentage area of FPGA

is not utilized in every configuration. As a result, the power dissipation of FPGA device is significantly larger than that of their ASIC counterpart. Thus, the large power consumption of FPGA has become a constraining factor for FPGA designs to enter main stream low power portable applications [19]. Field programmability and adaptability highlights of FPGAs are appealing notwithstanding for ULP applications [15]. Henceforth, it is vital to upgrade the speed of subthreshold FPGA so it can contend with ASICs being utilized in ULP frameworks.

In spite of the relative shortcoming of FPGAs from the leakage power point, very little research has been done on leakage power lessening in FPGAs. The earlier research work has been for the most part worried about unique power utilization [20] and accepts leakage energy to be a little segment of the aggregate power. In any case, these investigations depend on advances having hub of 0.15μm or above, making them to some degree out of venture with the present cutting edge FPGAs, which are created in sub-100nm innovation. International technology roadmap of semiconductors (ITRS) indicates that as technology reaches to smaller node, leakage will dominate the total power distribution [23].

Unlike ASICs, an FPGA circuit implementation uses only a fraction of FPGA resources. Leakage power is dispersed in both the utilized and unutilized parts of the FPGA [22]. In this manner, the leakage power utilization is higher than the dynamic power utilization. Further, the programmability of FPGA gathers that more transistors are required to realize a given method of reasoning circuit, in relationship with ASICs. Leakage power is with respect to mean transistor count, and along these lines, leakage upgrade will most likely be a key blueprint objective in future FPGA headways. Lessening the power use of FPGA is invaluable as it cuts down bundling/cooling cost, improves constancy and engages FPGA use in low-control reduced applications which could work at coordinate speed.

Interconnect fundamentally decides the execution at the nanoscale [12, 14]. Henceforth, the plan of interconnect is significant in upgrading the execution of VLSI circuits. Ideal subthreshold circuit execution is accomplished by gadget as well as circuit streamlining methods [16-17]. Further refinements are made to refine and enhance the speed of interconnects under subthreshold conditions [15, 18-19]. Accordingly, it is important to investigate distinctive materials copper (Cu), carbon nano-tube (CNT), graphene nano ribbon (GNR) and so forth for interconnects and

complete parameter advancement to accomplish best execution under subthreshold condition. The exponential connection amongst current and voltage in subthreshold administration makes subthreshold circuits more inclined to process-voltage-temperature (PVT) varieties [20]. Late investigations have shown that the decrease in V_{DD} expands the gadget weakness to process varieties, bringing about spreading of circuit outline measurements from their ostensible esteems and diminished commotion edge [16, 17]. Along these lines, while planning subthreshold circuits, it is fundamental to consider the vigor issue. It is normal that rising gadgets like Carbon Nanotube Field Effect Transistors (CNFET), Tunnel Field Effect Transistors (TFET) and Fin Field Effect Transistor (FinFET) will supplant the current mass Si-MOSFET innovation later on [21-23]. Consequently, it is important to examine and enhance the execution of subthreshold circuits utilizing TFET, FinFET and CNFET under subthreshold conditions. Thus, it is important to plan new gadget parameters to enhance the drive current to upgrade the speed of subthreshold circuits. While investigating rapid and vigorous subthreshold circuit plan, different commitments made in this postulation are talked about in the following area.

1.3 Contribution

Following are the key contributions made in this thesis while designing energy efficient FPGA architecture for moderate speed applications.

- This work, reviewed an upcoming emerging device type of transistor; Tunnel Field Effect transistors (TFET). The TFET is approximately closer to MOSFET, however, with different fundamental switching mechanism done by modulating quantum tunneling through a barrier instead of modulating thermionic emission over a barrier as in traditional MOSFETs. The work explored journey of TFET since its inception from Surface Tunnel Transistor to till date.
- Furthermore, this thesis explores the challenges being faced by conventional Al and Cu interconnects. Due to aggressive technology scaling, the Cu resistivity increases because of size effects, which causes increase in delay, power dissipation and electro-migration. The purpose of this component of research is to explore the interconnect material used in IC from introduction of ICs to till today. This work deals with studies and reviews new materials available for interconnect application which are OI,

CNT, GNR, and SiN which are alternatives to Cu. This literature relives that MWCNTs, MLGNR and MCBs are promising candidates that can strongly address the problems faced by Cu, however on integration basis Cu would last for coming years.

- The simulated performance comparison between MOSFET and TFET is carried out to explore the various facts of the two devices. It revealed that, TFET has lower SS than MOSFETs. TFET is applicable for low power devices as it gives lower I_{OFF}.
- This work also deals with the PNPN TFET in which gate controls the source to channel tunnelling current through modulation of BTBT. The hetero-gate dielectric structure is designed with the addition of a hetero-dielectric Buried Oxide on the doped substrate for reduction of ambipolar current and improvement of tunneling current at drain and source side respectively. Modeled PNPN TFET had resulted in improved performance in-terms of I_{ON}/I_{OFF} ratio, using low band gap material and hence is best alternative over the conventional MOSFET for the low power and moderate speed applications.
- Furthermore, this thesis proposes the comparison between MWCNT, MCB, and MLGNR interconnects incorporated with CNFET and TFET technologies. MLGNR shows lesser propagation delay, power dissipation, and PDP than the MWCNT and MCB interconnects; Hence, it is considered the best candidate to replace Cu interconnects in VLSI chips.
- Furthermore, this thesis analyzed that high resistivity of Cu interconnect is bringing on expansive defer and power utilization in the IC at global interconnect length. This work relives that, SWCNT is well appropriate for local interconnect whereas MWCNT and MCB are best reasonable for intermediate and global interconnect. However, for CNFET driver, MCB and MWCNT are appropriate for all level of interconnects compared to Cu interconnect technology.
- This thesis had successfully demonstrated the VCO designs using two different schematics viz. SCVCO and AVLGVCO. The proposed AVLG based SC-VCO indicates higher wavering frequencies than the conventional SC-VCO. This work analysed the input voltage, temperature

and gate length variations on oscillation frequency and average power respectively.

- In this work, differential amplifier is designed for parameters viz. Slew Rate, Gain, CMRR, Unity Gain Bandwidth and Frequency Response and its comparison with MOSFET, FinFET and CNFET is made. The simulation work proposes that the FinFET circuit performs best than the MOSFET and CNFET in terms of Gain, CMRR and Slew Rate.

1.4 Thesis Organization

The core chapters of this thesis, from Chapter 2 to Chapter 6, are a collection of literature review, manuscripts published in reputed journals, International Journals, IEEE Conferences and International Conferences. This thesis specially targets design of energy efficient FPGA and interconnects for moderate speed applications. The thesis is structured as follows:

Chapter 2 covers overview of literature review. The issues related to the low power techniques are presented here. FPGA Architecture is discussed in brief since from the inception of the FPGA architecture along with various different types of it like the Island and the low power architecture are explored here.

Chapter 3 proposes in brief survey on the TFET and Interconnects which is presented in detail. A detailed discussion is made on the challenges in the low power FPGA architecture in terms of interconnect level, device level and the circuit levels are discussed. This work is published in IJAER Journal and T&F International Journal of Electronics and other part is submitted to Scopus indexed IJEEI Journal which is presently under review. Various energy efficient Interconnect techniques along with the CMOS and post-CMOS devices are explored here which could work for the low power and energy efficient circuits.

Chapter 4 evaluates the performance of the emerging devices. This chapter explored the various simulations executed on the TFET based on the state of the art design considering the recent trends in the post-CMOS devices. The performance parameters are evaluated in terms of its ON current (I_{ON}), OFF current (I_{OFF}), Subthreshold swing (SS), Power delay product (PDP),

Transconductance (g_m) etc. Some part of this work is published in UGC Indexed IJST Journal and other is presented in International Conference.

Chapter 5 explores the performance of the emerging interconnects. This section explored the various simulations executed on conventional cu and compared the same with the emerging interconnects viz. single walled carbon nanotube (SWCNT), multi walled carbon nanotube (MWCNT), mixed carbon bundle (MCB), single layer graphene nano ribbon (SLGNR), multi-layer graphene nano ribbon (MLGNR) respectively. This section evaluated the performance in terms of the drivers specifically using CMOS, FinFET, TFET and CNFET devices. The performance parameters are measured for various lengths and parameters extracted in terms of PDP, Delay, Speed, and Power Dissipation (PD). A part of this work is presented and published in IEEE Conference and the other part is published in UGC Indexed IJST Journal.

Chapter 6 evaluates the performance of digital circuits. Various digital circuit schematics are explored and its performance is being measured and presented. The evaluation is done on the 6T SRAM Cell Design and Source Coupled Voltage Controlled Oscillator (SCVCO) schematics and counter designs. Part of the work is presented and is published in IEEE Conference.

Chapter 7 summarizes the entire work which had been executed in the thesis. It additionally reaches inferences and the rundown of the theory and proposes zones of future research work.

The next chapter reviews the low power techniques. It introduces a review of the wellsprings of energy utilization in CMOS, dynamic power lessening systems, spillage control decrease strategies. The details related to FPGA architecture is presented along with the details of the classifications are specified herein.

Chapter 2

LOW POWER TECHNIQUES AND FPGA ARCHITECTURE

As per the International Energy Agency (IEA), electronic gadgets at present record for 15% of family unit power utilization, and vitality devoured by data and correspondence innovations and in addition shopper hardware will twofold by 2022 and triple by 2030. Therefore, low-power electronics is not only mandatory for portable devices and future applications, like sensors for ambient intelligence and implantable bio-medical devices, but for all kinds of information processing devices. This chapter reviews the different low power techniques, FPGA architectures and Literature review etc.

Subthreshold operation is the most power efficient regime of operation in a transistor to ensure that systems are robust to transistor mismatch, power-supply-voltage noise, and temperature variations. Hence, one of the aspects of this research is to design robust circuits. This section presents wellsprings of energy dissemination in CMOS transistors with an extraordinary concentrate on those adding to the static power utilization. Section 2.1 reviews control scattering in CMOS circuits, covering both dynamic and static power. Section 2.2 specifies about the FPGA Architecture, 2.3 and 2.4 explores about the Structural Classification and on user programmable switch technologies, 2.5 deals with the major building blocks of FPGA and 2.6 mentions about the detailed literature review. Summary is mentioned in Section 2.7.

2.1 Low Power Techniques

2.1.1 Sources of Power Consumption in CMOS Circuits

The power consumption sources in CMOS integrated circuits (ICs) are classified as dynamic /switching power, short circuit power and static power.

A. Dynamic/Switching Power

The dynamic power consumption is the power consumed during charging and dis- charging of capacitances associated with each circuit node [24]. The components of dynamic power is shown in equation (2.1)

$$Pdy = \alpha FCV_{DD}^{2} \quad \text{..... (2.1)}$$

Where, power supply voltage is denoted as 'V_{DD}', 'F' as the clock frequency, and 'α' is the exchanging component (or movement factor). Condition (2.1) demonstrates that the power utilization is an element of the square of the supply voltage and thus the most critical decrease in power can be accomplished by lessening V_{DD}.

B. Short-Circuit Power

The second segment of energy utilization is the short out power. This power utilization is brought about when both pull-up and pull-down transistors are in ON condition. Consider the easiest static integral MOS (CMOS) inverter appeared in Fig. 2.1.When NMOS transistor turns ON because of a rising waveform at the information, at that point the PMOS transistor similarly on directing current until the point that the info voltage winds up noticeably more prominent than $V_{DD} - |Vtp|$, (henceforth the two transistors are ON at the same time). Therefore, a direct current flow from supply to ground, which is called short-circuit current [25]. The short-circuit current waveform can be approximated as a triangular wave. The aggregate charge that streams in this period can be found by ascertaining the zone of this triangle. Let 't_r' signifies the ideal opportunity for the information voltage to ascend from '*Vtn'* to $V_{DD}-|Vtp|$ where '*Vtn/Vtp'* are the limit voltages of NMOS/PMOS transistors individually. Expecting symmetric high-to-low and low-to-high changes for both info and yield of the rationale door, the aggregate short out power for a solitary rationale entryway is characterized as

$$P_{SC} = \alpha . t_r V_{DD} I_{peak} F \quad \text{.....(2.2)}$$

Where 'α' is the switching activity factor and 'I_{peak}' is the peak current per transistor width [26].

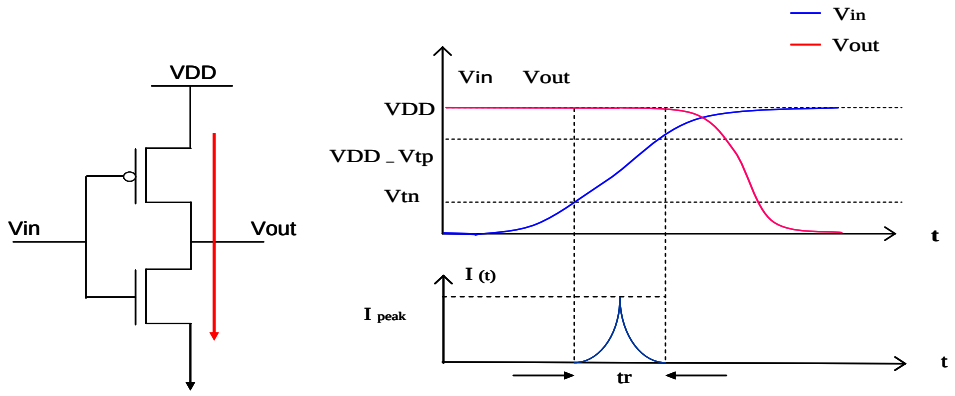


Figure 2.1: Schematic of inverter with voltage and current waveforms.

C. Static Power

The static power is characterized as the power utilization began from current continually spilling out of V_{DD} to ground. This implies notwithstanding when the circuit is out of gear mode (no movement), control keeps on being disseminated. For long channel transistors with high limit voltage, this kind of scattering was immaterial. Tragically, present and future advances will experience the ill effects of high static power, which could even surpass the dynamic commitment in dynamic mode. The contracting geometries have prompted diverse sources of leakage current. Fig. 2.2 demonstrates the distinctive spillage current instruments through a short channel NMOS transistor [27-29], for example

(a) Reverse bias p-n junction current and band to band tunneling (I_1)

(b) Subthreshold current (I_2)

(c) Gate Leakage current (I_3)

(d) Gate current due to hot-carrier injection (I_4)

(e) Gate-Induced Drain Leakage (I_5)

(f) Punch through (I_6)

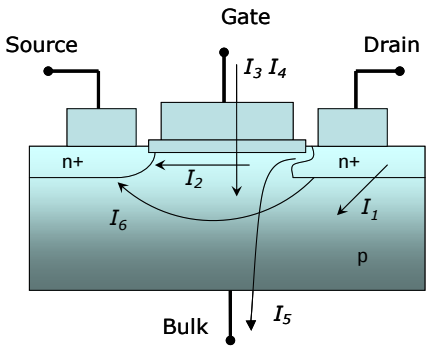


Figure 2.2: Leakage mechanisms in an NMOS Transistor.

In ordinary MOS transistor operation mode, the drain/source to well intersections is turn around one-sided, causing p-n intersection leakage current (*I1*). This current is made in light of the minority carrier diffusion / drift near the edge of the depletion area, and as a result of electron-opening pair age in the consumption area of the switch one-sided intersection [30-31]. The n and p regions areas are intensely doped by then band-to-band tunneling (BTBT) starts to manage the spillage current in the p-n junction.

The Subthreshold current (*I2*) is begun by the scattering of minority bearers in a non-coordinating transistor i.e. ($V_{GS} < V_{th}$). Under this condition, the MOS transistor is working in fragile inversion [32]. The subthreshold current has an exponential reliance on the edge voltage (V_{th}). This is the motivation behind why the low V_{th} portraying late innovations prompt substantial subthreshold current. By expanding the body potential in a NMOS or by diminishing it in a PMOS (forward biasing), the intersection exhaustion decreases as the limit voltage prompts the expansion in sub-threshold leakage current.

Similarly, a reduction in body potential increases the depletion charge and hence the V_{th}, leading to reduced subthreshold leakage [33-34].

The subthreshold leakage is given by [35]

$$Isub = \mu oCox\frac{W}{L}(V_T)^2 e^{1.8} e(\frac{V_{GS} - Vth}{nV_T})(1 - e\frac{-V_{DS}}{V_T}) \quad \text{.....(2.3)}$$

Where $m = 1 + \frac{Cdm}{Cox}$

Where 'μo' is the zero bias mobility, 'V_{th}' is the threshold voltage, 'V_T' is the thermal voltage, 'n' is the subthreshold swing coefficient, *'Cox'* is the gate oxide capacitance, '*Cdm*' is the capacitance of depletion layer and '*W/L'* is the width/length of transistor respectively.

It is clear from condition (2.3), that the lessening of V_{th} exponentially builds the subthreshold leakage current. Additionally diminishing the length of transistors unlike expands the subthreshold leakage. The gate leakage (*I3*) is because of direct tunneling current that enters the gate insulator. Not at all like subthreshold leakage, the gate leakage available in both the OFF state and the ON state of MOS transistor, which makes gate leakage harder to control than subthreshold leakage [36-37]. In the ON state, the gate leakage is the sum of two components namely the gate to channel and the gate to source/drain extension overlap current, while in OFF state, it is due to edge direct-tunneling current 'I_{EDT}'. Hence, the gate leakage strongly depends on the potential of transistor's gate 'V_G', gate oxide thickness '*Tox*', gate oxide material '*K*', and the width of the transistor '*W*'. The gate leakage expressed in [41] is given by equation 2.4.

$$Igate = WeffLeffA(\frac{Vox}{Tox})^2 \exp\left[\frac{-B(1-(1-\frac{Vox}{\phi ox})\frac{3}{2})}{\frac{Vox}{\phi ox}}\right] \quad \text{.....(2.4)}$$

$$A = \frac{q^3}{16\prod^2 h\phi ox} \qquad B = \frac{4\sqrt{2m}\,\phi ox^{3/2}}{3hq}$$

Where '*Vox'* is the potential drop across the thin oxide layer [14]; '*Ǿox'* is the barrier height for the tunneling particles, '*Tox*' is the oxide thickness, '*A*' and '*B*' are the physical parameters.

In the overlapping zone amongst gate and drain, a high electric field exists, prompting the age of current from drain to substrate. Consider a NMOS transistor; when a low gate potential is connected (VG≈0V), openings gather at the surface and make a region which is more intensely p-doped than the substrate. If this happens while the drain is connected to a high potential (say V_{DD}), the depletion layer near the drain becomes narrower. Thinner oxide thickness and higher potential amongst gate and drain upgrade the electric field and, along these lines, expands the Gate-Induced Drain Leakage (GIDL) [38-39].

As the channel length is diminished for a settled doping level, the partition between the depletion region limits diminishes. An increase in the reverse bias across the junctions (with increase in VDS) also pushes the junctions nearer to each other. When the combination of channel length and reverse bias leads to the merging of the depletion regions, punch through occurs.

2.1.2 Dynamic Power Reduction Techniques

The following techniques can be used to reduce the dynamic power

A. Dual Power Supply

Diminishing the supply voltage '*V*', or voltage scaling is the best technique for dynamic power dissipation 'P_{dy}', since dynamic power is comparing to the square of *V*. The system can fundamentally lessen disseminated control without degrading speed; by bringing down the *V* along non-basic postpone ways or light workloads and higher V for substantial workloads [40-41]. Fig. 2.3 shows the case of the same.

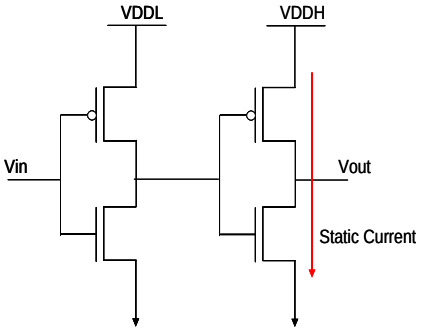


Figure 2.3: A low voltage inverter driving a high voltage inverter.

B. Decreasing Switched Capacitance

The most obvious strategy for dynamic power reducing is to take out inconsequential trading development in the circuit. Clock gating is the most by and large used strategy consequently. By gating the clock to particular flip-flops, the action in blocks is disposed OFF. Clock gating is a circuit-level procedure and it is generally connected near the finish of the plan procedure, so the advantages possible by this strategy are constrained. Procedures connected at larger amounts of deliberation, for example, compositional changes and additionally algorithmic changes can possibly diminish the unnecessary switching in the circuit.

C. Gate Sizing

Non-fundamental ways have timing slack and the delays of a couple of gates on these ways can be extended without impacting the execution. Since the length of gadgets (transistors) in a gate are regularly inconsequential for a quick application. The gate deferral can be extended by decreasing the device width; along these lines, the dynamic power is in like way reduced as a result of tinier stacking capacitance '*CL*', which is in respect to the device evaluate. Gate evaluating is a strategy that chooses device widths for gateways [42-43].

D. Transistor Sizing

The basic thought of transistor assessing is definitely the same as that of gate measuring beside that in gate measuring each one of the transistors in a solitary gate are measured together with a comparable factor however in transistor measuring each transistor can be measured self-governing, consequently transistor estimating [44-45] investigates the most extreme conceivable enhancement space for power reduction without much performance degradation.

2.1.3 Leakage Power Reduction Techniques

The following techniques can be used to reduce the leakage power

A. Power Gating and Multi-Threshold Voltage

A definitive method for decreasing the leakage power dissipation of a CMOS circuit in standby mode is to turn off its V_{DD}. The NMOS addition plot is ideal, since the NMOS R_{ON} is littler for a similar width; in this way, it can be estimated littler when contrasted with PMOS. The addition of these transistors makes a virtual ground and a virtual V_{DD} rail as portrayed in Fig. 2.4. In the ACTIVE mode, the lay transistor is ON, thusly, the circuit limits as anyone might expect whereas in the STANDBY mode, the transistor is OFF, which separates the circuit beginning from the earliest stage. Note that to cut down the leakage power, the edge voltage of the off transistor must be far reaching. Else, the OFF transistor will have a high leakage current which makes control gating less intense. Eventually, twofold V_{th} CMOS or Multi-Threshold CMOS (MTCMOS) is used for control gating [46-47]. In these progressions, there are a couple of sorts of transistors with different V_{th} regards. Transistors with a low V_{th} are used to execute the basis, while high V_{th} gadgets are used as OFF transistors.

To ensure legitimate usefulness of the circuit, the OFF transistor must be painstakingly estimated to diminish its voltage drop when it is ON. The voltage drop over the OFF transistor diminishes the compelling VDD of the rationale logic gate. This issue can be unraveled by utilizing an extensive OFF transistor. Since utilizing one transistor for every rationale logic gate brings about a vast territory and power overhead, one transistor might be utilized for a gathering of gates as delineated in Fig. 2.5. Notice that the traverse of the OFF transistor for this circumstance ought to be greater than the one used as a piece of Fig. 2.4. This requires recreating the circuit under all conceivable info esteems, an assignment that is unrealistic for extensive circuits. Nonetheless, it experiences the accompanying bad marks:

- It requires change in the CMOS development technique to help both a high V_{th} contraption (for OFF transistor) and a low V_{th} gadget (for logic gates).
- It decreases the voltage swing and in this way the DC noise margin.
- OFF transistor measuring is an important task and requires much effort.

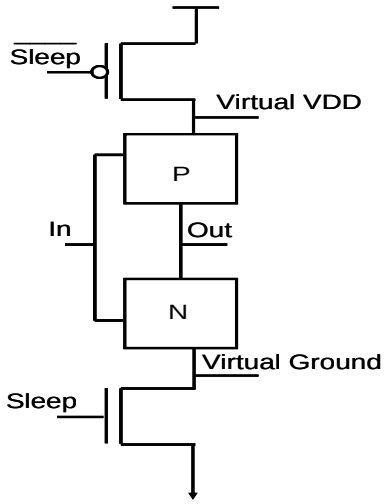


Figure 2.4: Schematic of Multi-Threshold CMOS inverter.

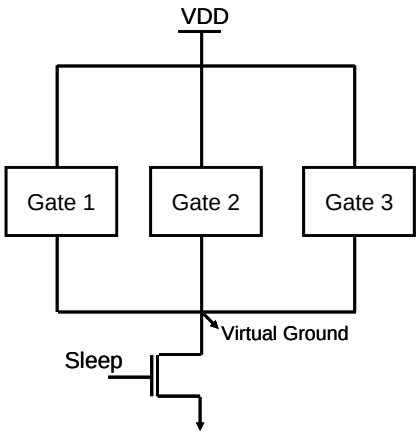


Figure 2.5: Schematic of common sleep transistor.

B. Adaptive Body Bias

One of the strategies for diminishing the leakage current is utilizing reverse body bias (RBB), to build the limit voltage of transistors in the STANDBY state [48]. The V_{th} of a transistor is given by the accompanying standard expression,

$$Vth = Vtho + \gamma(\sqrt{|-2\phi F + V_{SB}|} - \sqrt{|2\phi F|}) \quad \text{.....(2.5)}$$

Where '*Vtho*' is the threshold voltage for V_{SB}=0, *'ØF'* is the substrate Fermi potential and the parameter 'γ' is the body-effect coefficient. As obvious, reverse biasing a transistor builds its V_{th}. A compelling way to deal with diminish subthreshold leakage includes progressively changing the body predisposition of transistors [49-51]. Ordinarily, a square level approach is favored as it gives leakage control lessening at whatever point the practical piece winds up noticeably sit still, paying little respect to the operation of whatever is left of the chip.

A square schematic of this approach is appeared in Fig. 2.6. At the point when the body enters the standby state, turn around body inclination (RBB) is connected to build the V_{th} of transistors, which diminishes subthreshold leakage current. Be that as it may, the upside of this approach over the rest transistors is that it can be executed immediately punishment. This should be possible by applying forward body predisposition (FBB) when the piece is in the dynamic state. Under FBB, the V_{th} of gadgets is brought down, which enhances the execution.

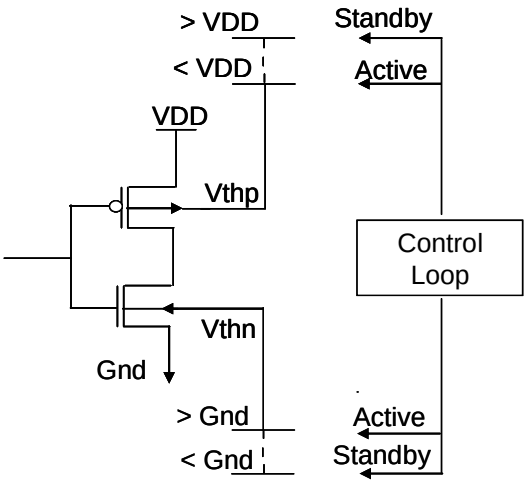


Figure 2.6: Adaptive Body Biasing.

C. Transistor Stacks

Subthreshold leakage current coursing through a heap of plan related transistors reduces when more than one transistor in the stack is turned OFF. This effect is known as the stacking impact [52-54]. The stacking impact in two-input NAND gate is appeared in Fig. 2.7. Right when the two transistors M1 and M2 are turned OFF, the voltage at the direct center point (VM) is sure. This is because of the little deplete current coursing through M1 and M2. Because of the positive capability of VM, the gate-to-source voltage (V_{GS}) of M1 winds up plainly negative thus, the subthreshold current diminishes significantly. Thus, because of VM, the body-to-source potential (VBS) of M1 winds up plainly negative, bringing about an expansion in the V_{th} of M1. With transistor stacking by supplanting one single OFF transistor with a heap of serially-related OFF transistors, leakage can be on a very basic level reduced. The disadvantage is that the pile of transistors causes either execution debasement or more special power use.

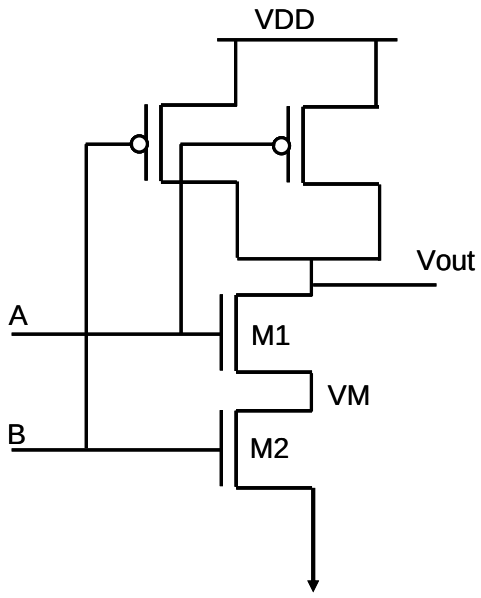


Figure 2.7: Stacking effect in two-input NAND gate.

D. Forced Transistor Stacking

Stack impact or self-reverse bias impact is where leakage current reduces because of at least two arrangement associated transistors turning OFF. Fig. 2.8 illustrates this concept.

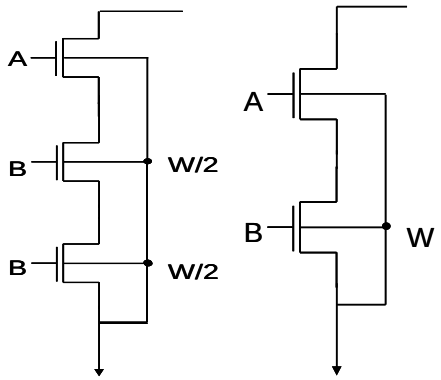


Figure 2.8: Forced stacking concept.

As the depth of the stack is expanded, higher leakage control sparing is watched. Although, in specific circuits the normal stacking of transistors does not exist. To use the stacking impact in such a circumstance, a solitary transistor of width '*W*' is supplanted by two transistors; every width is picked to *W/2*, which is called as constrained stacking. Since two transistors OFF in the meantime, stacking impact lessens subthreshold leakage current.

E. Sleepy Stack

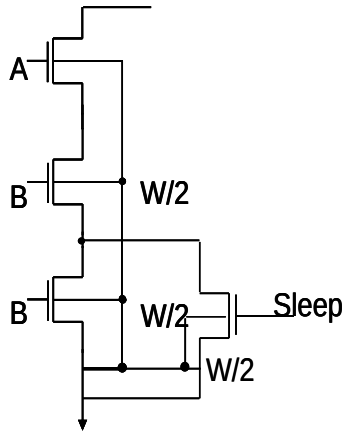


Figure 2.9: Sleepy stack concept.

In this method, forced stacking is first executed. At that point to one of the stacked transistors, a sleep transistor is associated in parallel as appeared in Fig. 2.9. Accordingly, in dynamic mode, sleep transistors are ON in this manner, decreasing the successful protection of the way. This prompts diminished spread postponement in dynamic mode when contrasted with the constrained stacking strategy. In standby mode, the sleep transistor is turned OFF and the stacked transistor smothers leakage.

F. Long Channel Devices

The dynamic leakage of CMOS circuits can be reduced by growing their transistor channel lengths. This is by virtue of there is a V_{th} get off in view of the Short Channel Effect (SCE). Particularly V_{th} can be refined by using different channel lengths. The more drawn out channel length is utilized to accomplish high limit voltage which expands the gate capacitance; subsequently, it negatively affects the execution and dynamic power dissemination. Long channel incorporation has near or brings down process cost, taken as the size augmentations instead of the take care of expense [52]. Moreover, unique channel lengths track each other over process variety. The strategy can be connected in a voracious way to a current outline to restrict the leakage current [57].

G. Optimal Standby Vector

Subthreshold leakage current relies upon the vectors connected to the gate inputs in light of the fact that diverse vectors make distinctive transistors be turned OFF. For instance, a 2-input NAND gate has the littlest subthreshold leakage because of the stacking impact when the information vector is ‘00’. At the point when a circuit

is in the standby mode, one could precisely pick an information vector and let the aggregate leakage in the entire circuit be limited.

2.2 FPGA Architecture

A FPGA is a gadget that contains a network of reconfigurable gate array logic hardware. At the point when a FPGA is arranged, the internal hardware is associated in a way that makes an equipment usage of the product application. FPGAs are really parallel in nature so unique preparing operations don't need to go after similar assets. in any case, not under any condition like hard-wired printed circuit board designs which have settled gear resources, FPGA-based systems can really rewire their inside equipment to allow reconfiguration after the control structure is sent to the field. FPGA gadgets pass on the execution and reliability of submitted hardware equipment.

A singular FPGA can supplant a considerable number of discrete fragments by uniting countless logic gates in a single integrated circuit (IC) chip. The internal resources of a FPGA chip include a system of configurable logic blocks (CLBs) enveloped by an edges of I/O squares showed up in Fig. 2.10. Signals are steered inside the FPGA network by programmable interconnect switches and wire routes. in a FPGA logic blocks are actualized utilizing various level low fan-in gates, which gives it a more minimal plan contrasted with a usage with two-level AND-OR logic. FPGA provides its user a way to configure:

- The intersection between the logic blocks and
- The function of each logic block.

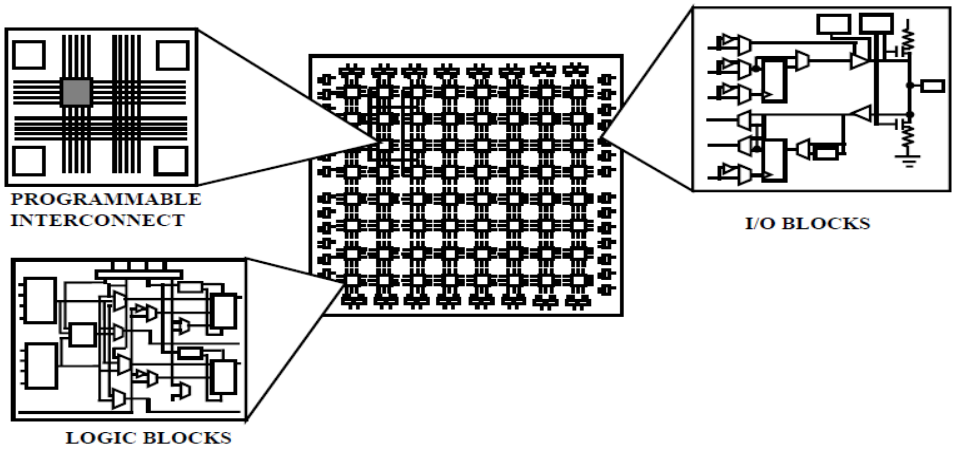


Figure 2.10: Internal structure of FPGA programmable interconnect logic blocks, I/O blocks.

Logic blocks of a FPGA can be designed such that it can give practicality as basic as that of transistor or as sophisticated as that of a microchip. It can have used to actualize distinctive mixes of combinational and consecutive logic capacities. Logic blocks of a FPGA can be executed by any of the accompanying:

- Transistor sets, Multiplexers.
- Combinational gates like fundamental NAND gates or XOR gates.
- n-input Lookup tables with Wide fan-in AND-OR structure.

Directing in FPGAs comprises of wire sections of differing lengths which can be interconnected through electrically programmable switches. Thickness of logic blocks utilized as a part of a FPGA relies upon length and number of wire sections utilized for directing. Number of fragments utilized for interconnection ordinarily is an exchange off between thickness of rationale squares utilized and measure of region spent for steering. Disentangled variant of FPGA inner engineering with directing is appeared in Fig. 2.11.

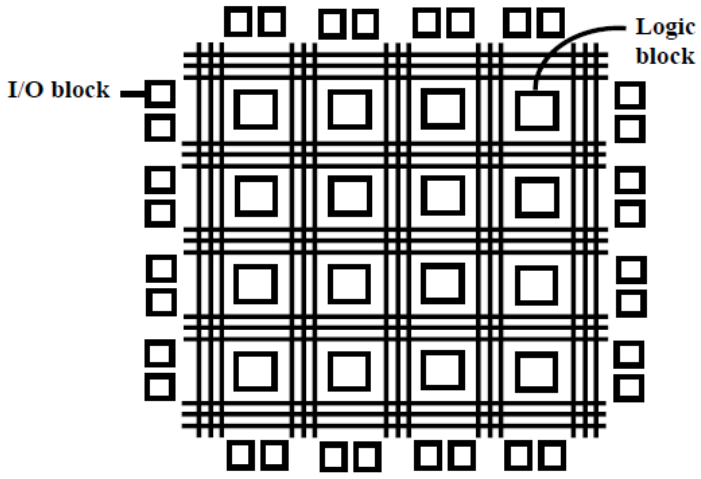


Figure 2.11: Simplified internal structure of FPGA logic block, I/O block.

Evaluation of FPGA

In the realm of computerized electronic frameworks, there are three essential sorts of devices: memory, microchips, and logic. Memory gadgets store arbitrary data, for example, the substance of a spreadsheet or database. Chip executes programming directions to play out a wide assortment of undertakings, for example, running a word preparing system or computer game. Logic devices give particular capacities, including device-to-device interfacing, information correspondence, flag preparing,

information show, timing and control operations, and practically every other capacity a framework must perform [56].

The principle kind of customer programmable chip that could execute logic circuits was the Programmable Read-Only Memory (PROM), in which address lines can be used as logic circuit information sources and information lines as yields. PROMS are in this way a wasteful engineering for acknowledging logic circuits, as are once in a while utilized as a part of training for that reason. Consistently, a PLA is a circuit that permits actualizing Boolean capacities in SOP form. The input buffer gives both the first and the modified estimations of every PLA input [61]. The information lines run on a level plane into the AND grid, while the supposed item term lines run vertically. In this manner, the span of the AND framework is double the quantity of sources of input times the quantity of POS.

At the point when PLAs were presented in the mid-1970s, by Philips, their primary disadvantages were that they were costly to make and offered to some degree poor speed-execution. The two burdens were a direct result of the two levels of configurable logic, in light of the fact that programmable logic planes were difficult to create and displayed huge propagation delays. To beat these shortcomings, Programmable Array Logic (PAL) devices were created. PALs give only a singular level of programmability, involving a programmable ‘wired’ AND plane that sustains settled OR-gates. PALs generally contain flip-flops related with the OR-gate yields so progressive circuits can be made sense of it. These are frequently alluded to as Simple Programmable Logic Devices (SPLDs). Fig. 2.12 demonstrates a streamlined structure of PLA and PAL with the progression of innovation, it has turned out to be conceivable to deliver devices with higher limits than SPLD's. As chip densities expanded, it was normal for the PLD makers to advance their items into bigger (sensibly, yet not really physically) parts called Complex Programmable Logic Devices (CPLDs).

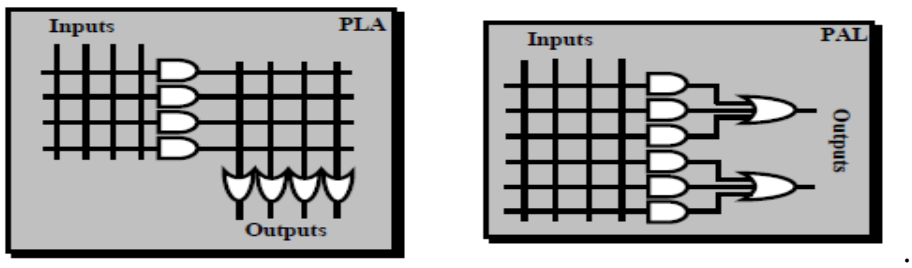


Figure 2.12: Simplified structure of PLA and PAL.

2.3 FPGA Structural Classification

Basic structure of a FPGA joins logic parts, programmable interconnects and memory. Game plan of these pieces is specific to particular creator. Introduction of inside strategy of pieces FPGAs can be segregated into three classes:

2.3.1 Symmetrical arrays

This engineering includes logic components (called CLBs) orchestrated in lines and sections of a system and interconnect laid out between them showed up in Fig. 2.16. This symmetrical system is incorporated by I/O pieces which relate it to outside world. Each CLB contains n-input Lookup table and a few programmable flip disappointments. I/O squares also control limits, for instance, tri-state control, and yield advance speed.

2.3.2 Row based architecture

Row based plan showed up in Fig. 2.13 contains trading segments of logic modules and programmable interconnect tracks. I/O blocks are arranged in the edges of the rows. One segment may be related with neighboring lines through vertical interconnect. Mix modules contain simply combinational parts which Sequential modules contain both combinational segments close by flip lemon. This progressive module can realize complex combinatorial-continuous

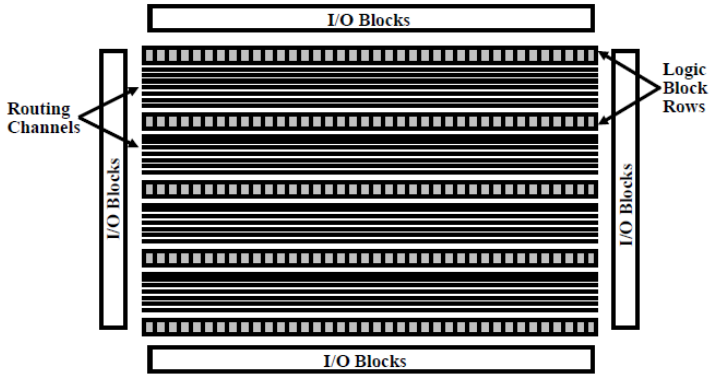


Figure 2.13: Row based Architecture.

2.3.3 Hierarchical PLDs

This design is arranged in different leveled route with top level containing just logic blocks and interconnects. Each logic block contains number of logic modules. Likewise, every logic module has combinational and moreover progressive practical parts. Each of these practical segments is controlled by the adjusted memory.

Correspondence between logic blocks is accomplished by programmable interconnects exhibits. I/O blocks encompass this plan of logic blocks and interconnect. This sort of engineering is appeared in Fig. 2.14.

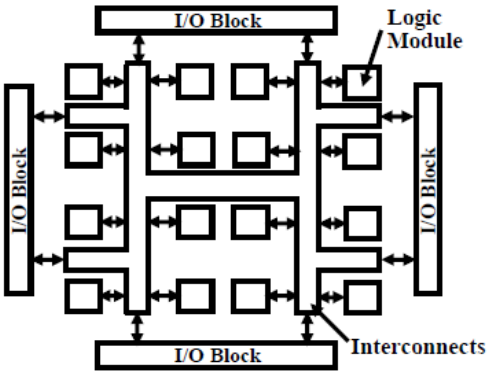


Figure 2.14: Hierarchical PLD.

2.4 FPGA Classification on user programmable switch technologies

FPGAs depend on a variety of logic modules and a supply of uncommitted wires to course the signals. In gate array these wires are associated by a cover outline amid fabricate. In FPGAs, however these wires are associated by the client and in this way should utilize an electronic device to interface them. Three sorts of devices have been generally used to do this, pass transistors controlled by a SRAM cell, a blaze or EEPROM cell to pass the flag, or a direct interface utilizing antifuse. Each of these interconnect devices have their own focal points and weaknesses. This majorly affects the outline, engineering, and execution of the FPGA. Grouping of FPGAs on client programmable switch innovation is given in Fig. 2.15 demonstrated as follows.

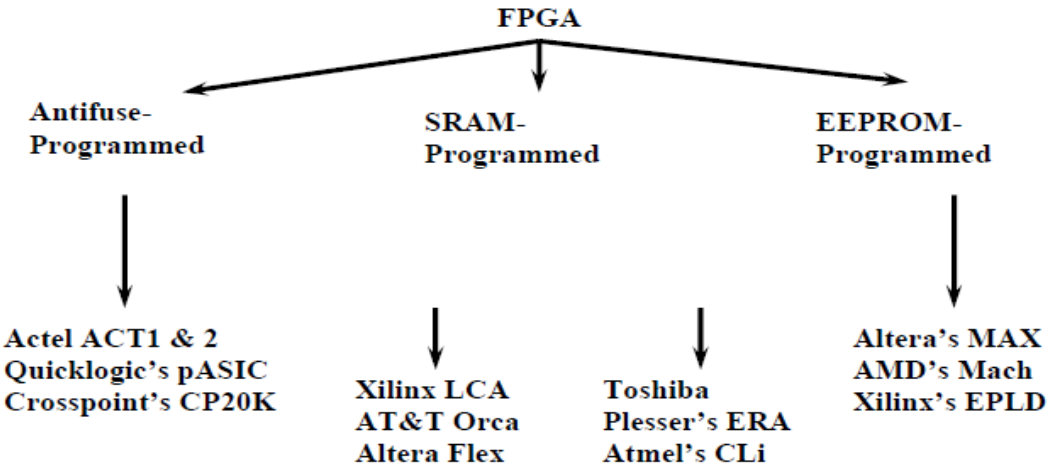


Figure 2.15: FPGA classification on user programmable technology.

2.4.1 SRAM Based FPGA

The real favorable position of SRAM based device is that they are boundlessly re-programmable and can be welded into the framework and have their capacity changed rapidly by simply changing the substance of a PROM. They along these lines have basic advancement mechanics. They can likewise be changed in the field by transferring new application code, a component alluring to planners. It does however accompany a cost as the interconnect component has high impedance and capacitance and in addition devouring considerably more territory than different innovations. Henceforth wires are exceptionally costly and moderate.

Fig. 2.16 shows two uses of SRAM cells: for controlling the gate nodes of pass-transistor changes and to control the select lines of multiplexers that drive logic block inputs. The figure give an instance of the relationship of one logic block (spoke to by the AND-door in the upper left corner) to another through two pass-transistor switches, and after that a multiplexer, all controlled by SRAM cells. Notwithstanding whether a FPGA uses pass-transistors or multiplexers or both depends upon the particular thing.

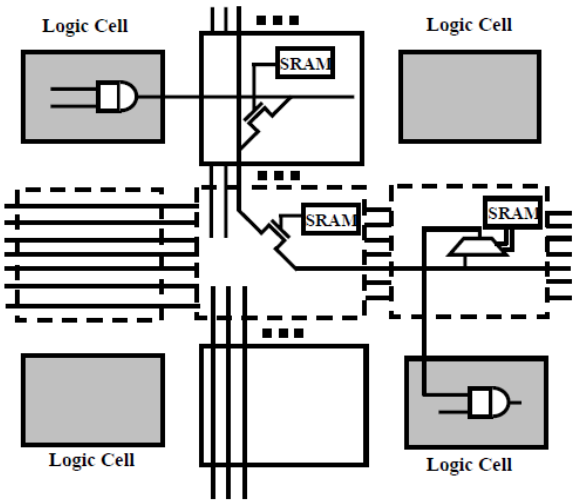


Figure 2.16: SRAM-controlled programmable switches.

2.4.2 Antifuse Based FPGA

The antifuse based cell is the most astounding thickness interconnects by being a genuine cross point. Subsequently the creator has a considerably bigger number of interconnects so logic modules can be littler and more productive. Place and course programming additionally has a considerably less demanding time. These

devices however are just a single time programmable and subsequently must be tossed out each time a change is made in the outline. The Antifuse has a characteristically low capacitance and protection with the end goal that the speediest parts are all Antifuse based. The detriment of the antifuse is the prerequisite to coordinate the manufacture of the antifuse into the IC procedure, which implies the procedure will dependably slack the SRAM procedure in scaling.

Antifuse are appropriate for FPGAs in light of the fact that they can be constructed utilizing altered CMOS innovation. For example Actel's antifuse structure is depicted in Fig. 2.17 exhibits that an antifuse is arranged between two interconnect wires and physically contains three sandwiched layers: the best and base layers are conveyors, and the middle layer is an insulator. At the point when un-modified, the encasing disengages the top and bottom layers, yet when customized the cover changes to wind up noticeably a low-protection connect. It utilizes Poly-Si and n+ dissemination as conductors and ON as insulator but other antifuse relies on metal for conductors, with amorphous silicon as the middle layer.

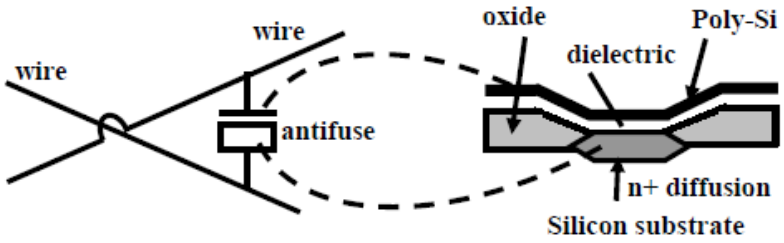


Figure 2.17: Actel Antifuse Structure.

2.4.3 EEPROM Based FPGA

The EEPROM/FLASH cell in FPGAs can be utilized as a part of two routes, as a control device as in a SRAM cell or as a specifically programmable switch. At the point when utilized as a switch they can be exceptionally effective as interconnect and can be reprogrammable in the meantime. They are additionally non-unstable so they don't require an additional PROM for stacking. FPGAs offer the most noteworthy measure of rationale thickness, the most highlights, and the most noteworthy execution. These propelled devices additionally offer highlights, for example, worked in hardwired processors, (for example, the IBM Power PC), considerable measures of memory, clock administration frameworks, and support for a significant number of the most recent quick device to-device signaling advances.

FPGAs are utilized as a part of a wide assortment of uses extending from information preparing and capacity, instrumentation, media communications, and advanced signal processing. As CPLD providers keep on integrating more capacities inside their devices, lessen expenses, and increment the accessibility of efficient IP centers, programmable logic is sure to extend its prominence with advanced originators.

2.5 Major Building Blocks of FPGA

Look Up Table

A Look up Table (LUT), is fundamentally a table that figures out what the yield is for any given input(s). With regards to combinational logic, it is truth table. This fact table successfully characterizes how your combinatorial logic carries on. P. S. Nair et.al [56] considered the leakage power in a SRAM bunch of FPGAs LUT for a 65nm CMOS process. The power-gating of a SRAM group of LUTs is executed both at coarse-grain and fine-grain levels. At to begin with, the leakage power scattering in a solitary SRAM cell was surveyed with and without control gating. By then, the leakage power dispersal in a 16:1 SRAM display was inspected for three cases: no power-gating, fine-grain control gating, and coarse-grain control gating. In fine-grain control gating, each SRAM cell is control gated independently however, for coarse-grain control gating, the entire display is control gated using one overall gating transistor, as showed up in Fig. 2.18. This display is the wellspring of data commitments for 16:1 multiplexer used as a piece of a LUT of FPGAs. It was found that more leakage reserve funds were obtained with coarse-grain control gating than with fine-grain control gating. The coarse-grain and fine-grain control gating methods yielded around 99% and 81% leakage speculation supports separately, completed the circumstance where no power gating was associated.

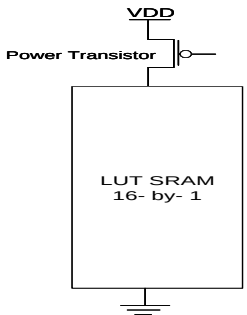


Figure 2.18: Coarse-gated SRAM cluster with 16 SRAM cells [57].

Mostafizur Rahman et.al [58] proposed another eccentric memory configuration called Tunnel FET based Random Access Memory (TNRAM) that enlightens CMOS SRAM scaling challenges through coordination of ultra-low power Tunnel FETs (TFETs) in a novel circuit style. Descriptive projections show gigantic power benefits; 6T-TNRAM has 4.38X lower dynamic power and 174X lower leakage control over HP 6T-SRAM at 16nm development center point.

Arifur Rahman et.al [60] suggested that each programmable logic and interconnection resource like LUT or controlling multiplexer can be control gated independently or any unused programmable resource can be set in rest mode, provoking lower dynamic leakage control usage. Fine-grain control gating gives more prominent controllability yet realizes the most essential zone overhead. Along these lines, coarse-grain control gating can be used by sharing the slept transistors among various similar programmable logic and interconnection resources, for instance, CLBs, LUTs and interconnection multiplexers (mux) etc.

SRAM

SRAM-based FPGA stores logic cells outline data in the static memory (cluster of locks). Since SRAM is erratic and can't keep data without control source, such FPGAs must be tweaked (orchestrated) upon start. There are two basic techniques for programming:

- Master mode, when FPGA peruses setup information from an outside source, for example, an outer Flash memory chip.
- Slave mode, when FPGA is designed by an outside master gadget, for example, a processor.

This can be for the most part done by methods for a dedicated plan interface or through a breaking point check (JTAG) interface. The researchers in [60, 61] reported the leakage power of FPGA device utilizing point by point circuit-level simulations. The simulation procedure represents plan subordinate varieties and gives itemized leakage power breakdowns. The leakage examination is based for the gathering of 1.2V, SRAM-based FPGAs worked in a 90nm CMOS process. The CLB setup is parceled into smaller circuit pieces. The total leakage power of the FPGA is measured by taking the aggregate of each piece's leakage power and after that expanded by the amount of CLBs in the assortment of that FPGA.

As leakage power of a circuit depends upon the estimations of its info sources, as needs be to demonstrate the impacts of input data, each circuit piece is reenacted under all possible data states, for instance, (min., max., and avg.). The base, most outrageous and ordinary leakage regards for all circuit discourages summed to enlist the total CLB leakage control for best-case, most cynical situation and typical case design data independently. In a FPGA, the three most consistent circuit sorts are plan SRAM cells, interconnect multiplexers, and LUTs. Fig. 2.19 exhibits the circuit-based leakage breakdown for an ordinary layout at 25°C. Joined, these three circuit sorts consume 88% of the total leakage power.

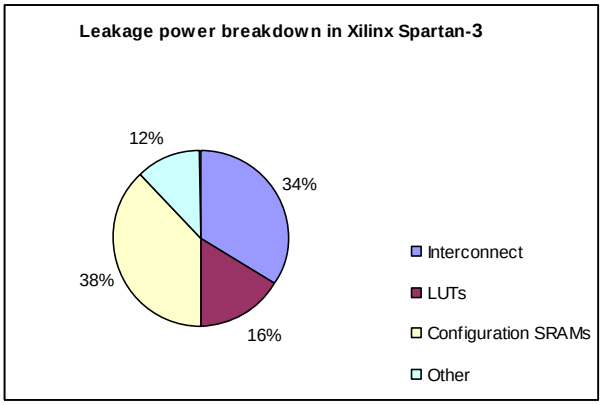


Figure 2.19: Leakage power breakdown based on circuit types [60].

Dual V_{DD} – Subthreshold

Dual V_{th} plot is a regular methodology for lessening leakage power in above-edge circuits. This exploration demonstrates that it is likewise powerful in lessening energy per cycle of sub-threshold circuits. In any case, in a double V_{th} design, the vitality per cycle depends upon both edge voltage and supply voltage. This section proposed a structure to additionally decrease energy per cycle underneath what is conceivable with a solitary V_{th}.

A programmable double V_{DD} structure for the CLB and the routing switch as proposed in [59, 62] communicated that the V_{DD} of the logic and routing blocks are changed by using configurable transistors as showed up in Fig. 2.20. Enormous power decreasing can be refined by distributing low- V_{DD} (V_{DDL}) to non-essential ways and high- V_{DD} (V_{DDH}) to the planning basic ways in the diagram to meet arranging objectives. Regardless, setting the '*LC'* at CLB yield pins diminishes the zone discipline by around 2% and still extras around 57% of total power. In light of the

zone overhead of LC and configurable supply transistors, the twofold V_{DD} FPGA takes around 21% more zone than a standard single- V_{DD} FPGA.

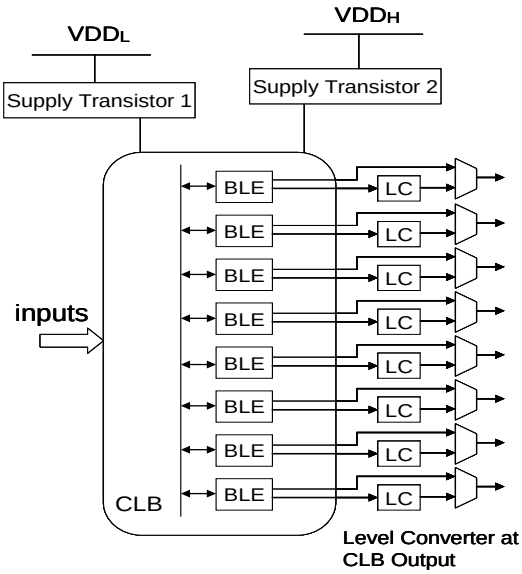


Figure 2.20: Dual-V_{DD} Assignment [60, 61].

2.6 Literature Review

FPGAs are promising answers for overseeing expanding plan intricacy while accomplishing both execution and adaptability. To support reconfiguration, FPGAs use more transistors per function than fixed-logic solutions, resulting in higher leakage power consumption. In this way, FPGAs are for the most part not found in portable applications. FPGA look into space has experienced an emotional advancement in the recent decades. Customarily, explore on FPGA CAD and engineering has principally centered on territory, productivity and execution. Nonetheless, ULP utilization is relied upon to be a key objective while planning future FPGAs to oblige the up and coming ULP advertise.

To rival low power ASICs, various examinations have been completed for lessening the dynamic and in addition leakage power utilization of FPGA in super threshold region. Bita Nezamfar and M. Horowitz [53] proposed beat mode interconnect procedure to improve the speed by 2X with minor power dispersal. Jason Cong and Bingjun Xiao [54] presented a novel FPGA engineering with resistive random access memory (RRAM) - based programmable interconnects (FPGA-RPI). Results demonstrated that the programmable interconnects of FPGA-RPI have a 96% littler impression, 55% higher execution, and 79% lower control utilizations contrasted with other FPGA partners.

Moreover A. Rahman et.al [64] utilized high V_{th} gadgets in unutilized directing and association switches alongside the self-changing V_{th} method to diminish the leakage current by 2 to 4X with 15%-30% region punishment. J. H. Anderson and F. N. Najm [09] proposed a routing switch having three distinctive working modes to be specific fast, low power or sleep mode and essentially diminished the leakage power dissipation by 28%-52% [63]. F. Li et.al. [62] proposed dual- V_{DD} FPGA design in which some logic blocks are settled to work at higher V_{DD} (rapid) and the others to work at bring down V_{DD} (low power). Fei. Li et.al [65] announced that FPGA regularly scatters just about 60%-70% power in interconnect texture (e.g. wires, association boxes, directing switches and supports), 10% to 20% in the clock system and 5%-20% in logic.

Further while focusing towards the reconfigurable compact devices B. H. Calhoun et.al [07] tended to about the execution bottlenecks forced by interconnect assets in future subthreshold FPGA. The execution breakdown demonstrates that in subthreshold FPGA interconnect assets expend 70% of aggregate vitality and gives 84% of aggregate postponement. As appeared in Fig. 2.21, interconnect organized keeps on ruling the general FPGA execution measurements under subthreshold conditions. In a similar work, creators likewise investigated the impact of PVT minor departure from defer execution of interconnect interface and is appeared in Fig. 2.22.

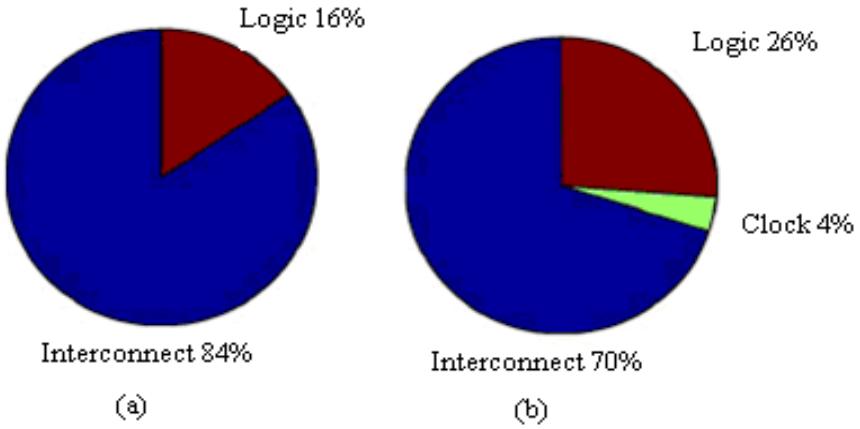


Figure 2.21: Breakdown of (a) delay (b) energy in simulation of FPGA at 0.4V Subthreshold Voltage [7].

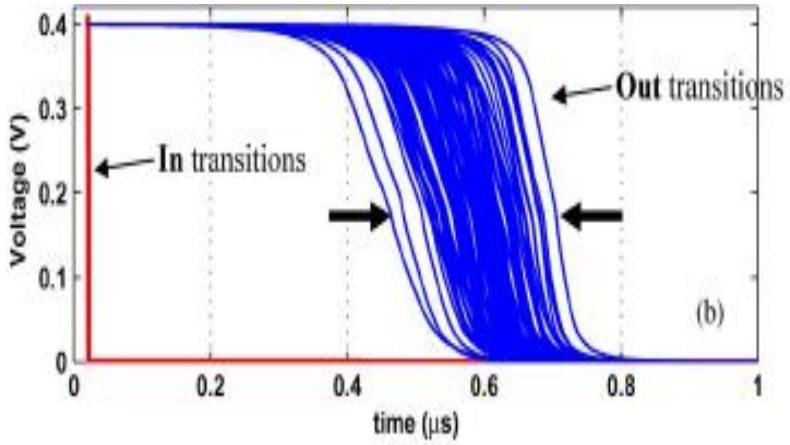


Figure 2.22: Monte Carlo simulation window for delay variation [7].

Moreover, J. F. Ryan and B. H. Calhoun [66] proposed low swing dual V_{DD} interconnect method for 90 nm subthreshold FPGA with 1134 LUTs. The proposed subthreshold FPGA is 2.7X littler, 14X speedier, and devours 4.7X less vitality than the subthreshold FPGA utilizing regular interconnects and 22X less vitality than a proportionate FPGA worked at ostensible V_{DD}.

The researchers in [60, 61] broke down the leakage power of FPGA gadget utilizing itemized circuit-level reenactments. The reproduction approach represents outline subordinate varieties and gives point by point leakage power breakdowns. in a FPGA, the three most normal circuit sorts are setup SRAM cells, interconnect multiplexers, and LUTs. Fig. 2.23 demonstrates the circuit-based leakage breakdown for a normal plan at 25°C. Consolidated, these three circuit sorts expend 88% of the aggregate leakage power.

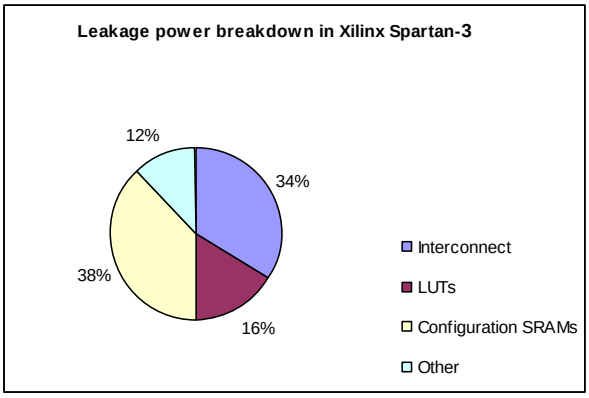


Figure 2.23: Leakage power breakdown based on circuit types [61].

J. H. Anderson et.al [67] proposed a plan of a routing switch for FPGA that is programmable to work in three distinct modes in particular rapid, low-power and sleep. To help diverse operation modes, the switch incorporates NMOS (MNX) and

PMOS (MPX) sleep transistors in parallel appeared in Fig. 2.24. As the yield swing is diminished by V_{th}, thusly, the exchanging vitality and leakage power are lessened significantly. In the sleep mode, both MPX and MNX are turned off, which is like supply gating.

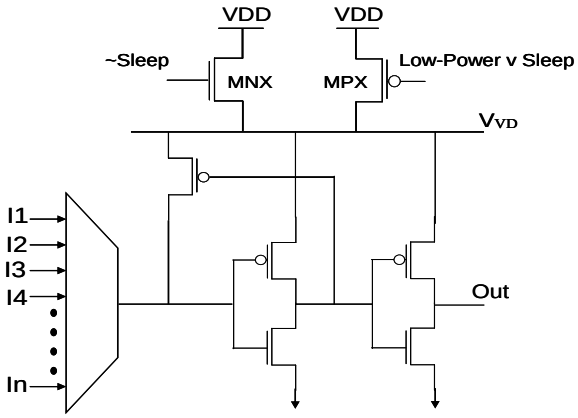


Figure 2.24: New programmable low-power FPGA routing switch [67].

Results demonstrate that the proposed switch configuration decreases leakage power utilization by up to 40% in low-control mode contrasted and fast mode, dynamic power by up to 28% and leakage power in sleep mode is 61% lower than that of rapid mode. Benton H. Calhoun et.al [68] proposed a plan approach utilizing gate level sleep gadgets and gave an intensive examination of sneak leakage ways in FPGA.

2.7 Summary

This section has presented the field of low power plan. Different procedures to decrease control utilization at the transistor level are depicted. Power dissemination in CMOS circuits can be either unique or static (leakage). Not at all like dynamic power utilization, does the leakage current also not rely upon the exchanging action. It just relies upon the quantity of transistors on the chip. The dynamic power has overwhelmed control utilization in CMOS circuits; in any case, innovation scaling patterns have brought about leakage turning into a prevailing segment of aggregate power. The architecture of FPGA with its Structural and user programmable switch technologies are also briefly discussed. FPGA building blocks are also elaborated and the literature survey is reported. The next chapter deals with the conventional CMOS and its counterpart emerging devices.

Chapter 3

DEVICES AND INTERCONNECTS

An IC is a set of electronic circuits on one small plate (‘chip’) of semiconductor material. Since the creation of the IC in 1960, Aluminum (Al) has become the primary material for interconnecting lines, and silicon dioxide (SiO_2) as the between level and intra-level insulator. The width of interconnects in a circuit is becoming smaller and smaller as the technology advances, rising resistivity and electro-migration problems. Metallic conductivity and resistance to electro-migration of bulk Cu were known to be better than those for Al which was the interconnect material until Cu interconnect was introduced in 1997.

As the strong innovation scaling proceeds with Cu interconnect resistivity increments because of surface harshness and grain limit dispersing, causing increment in propagation delay, power dissipation and electro-migration. Since last decade, several low power CMOS design techniques have been investigated that include device and/or circuit optimization. The most commonly used techniques for power reductions are transistor sizing, power gating, multi-V_{DD} approach, multi-threshold architectures, clock gating and supply voltage scaling. Various Post CMOS devices are reported in recent years. A detailed review of the same is also reported for TFET.

3.1 Interconnect for FPGA

The role of interconnects is to enable effective passing of clock and other signals in addition to providing power to various parts of chip.

A) Types of interconnect:

In current nanoscale regime, interconnects are categorized in three layers as per their lengths: local, intermediate, and global.

1) **Local:** It comprises of thin lines associating gates and transistors inside an execution unit or a functional block on the chip. Nearby wires for the most part traverse few gates and possess first and at times second metal layers in a multi-level framework. The lengths of these wires tend to downsize with innovation.
2) **Semi-global/Intermediate:** It gives clock and signal distribution inside a functional block with run of the mill lengths up to 100 to 500µm. Intermediate

wires are more extensive and taller than neighborhood wires to give bring down protection signal/clock paths.

3) **Global:** It gives clock and signal conveyance between the functional blocks, and conveys power/ground to all capacities on a chip. Global wires, which involve the best maybe a couple layers, are longer than 500 µm and can be the length of half of the chip border.

The first and second layers of interconnects from the best are global, the third and fourth layers are semi-global/intermediate, and the most minimal layers are local. Interconnects are stacked with dielectric material between two layers or between one layer to transistor, as appeared in Fig. 3.1.

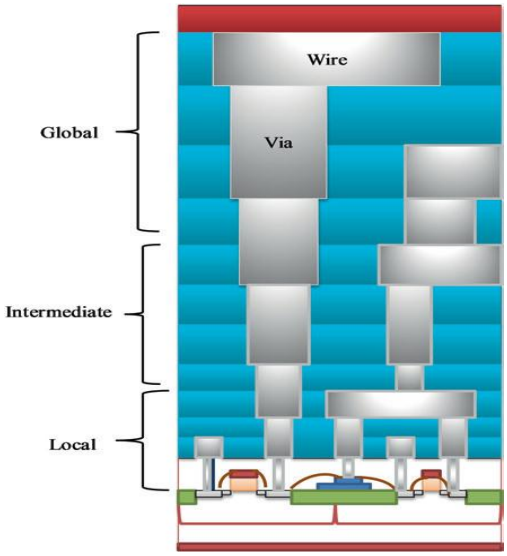


Figure 3.1: Cross section of stacked interconnects [69].

B) Interconnect Design Criteria:

Since, interconnect has turned into a prevailing issue in superior ICs, the concentration of the circuit configuration process has moved from logic improvement to interconnect enhancement. Criteria, for example, delay, power dissipation, noise, bandwidth, and physical zone ought to be considered for plan [69].

Delay:

Interconnect delay is an essential outline model because of the close relationship to the speed of a circuit. Early interconnect outline approaches concentrated essentially on delay optimization. A regular information way in a synchronous computerized circuit is appeared in Fig. 3.2. On account of zero clock skew, the base suitable clock time frame is

$$T_{p\_min} = T_{C\_Q} + T_{int} + T_{logicmax} + T_{setup} \quad \text{.....(3.1)}$$

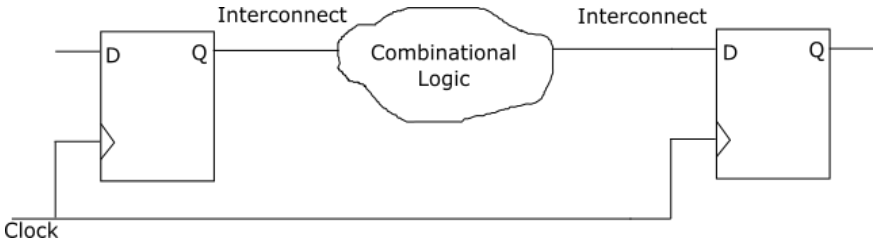


Figure 3.2: A data path in a synchronous digital system [70].

Where 'T_{C_Q}' is the time required for the data to leave the initial register after the clock signal arrives, 'T_{int}' is the interconnect delay, '$T_{logicmax}$' is the maximum logic gate delay, and 'T_{setup}' is the required setup time of the receiving register. From (interconnect logical), by reducing T_{int}, the clock period can be decreased, increasing the overall clock frequency of the circuit (assuming the data path is a critical path). By reducing the interconnect delay, the speed of the system, i.e., the computational efficiency of the cores can be improved at the architecture level.

Power dissipation:

Because of higher clock frequencies and on-chip mix levels, power dissipation has essentially expanded. The on-chip power dissipation of current cutting edge microchips is on the request of many watts and the power thickness has surpassed the power thickness of a kitchen hot plate [70]. In Fig. 3.3 power-sharing, the segments of dynamic power because of various capacitance sources are appeared.

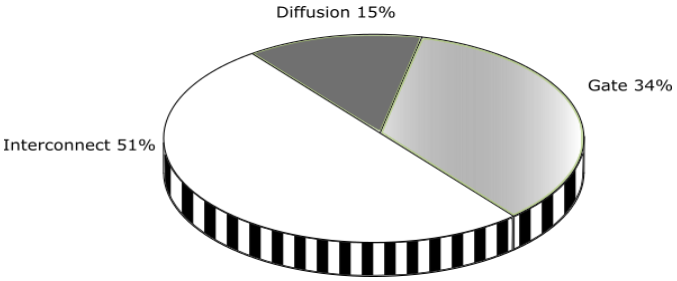


Figure 3.3: Components of Dynamic Power dissipation due to different capacitance sources: Gate capacitance, Diffusion capacitance, and Interconnect capacitance [70].

Dynamic power due to the interconnect capacitance can be more noteworthy than half of the aggregate dynamic power. Besides, the repeaters and pipeline registers embedded in interconnects present extra unique, leakage, and short out power. Power dissipation, accordingly, is another essential model in interconnect outline.

Noise:

With interconnect scaling, coupling capacitance between interconnects rules the ground capacitance. Besides, inductive coupling must be considered because of expanding signal frequencies, making coupling clamor more noteworthy. Interconnect coupling initiated noise can be arranged into two classes: voltage level noise and delay vulnerability, as appeared in Fig. 3.4 interconnect-coupling [70].

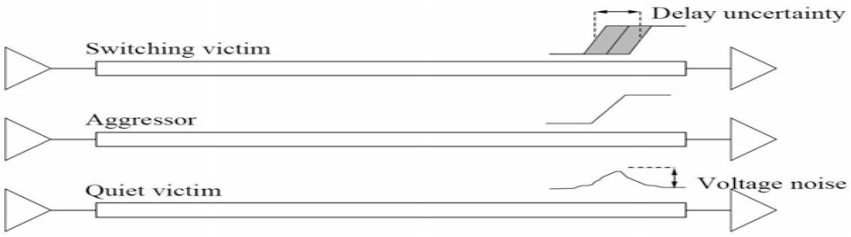


Figure 3.4: Interconnect coupling noise [71].

Physical Area:

With innovations in scaling, billions of transistors would now be able to be coordinated onto a single monolithic die. The die size, in any case, is relied upon to remain around settled for future innovations. The quantity of metal layers, in this way, should be expanded to give adequate metal assets to interconnect steering. Expanding the quantity of metal layers, be that as it may, builds the creation cost. The range measure, in this way, ought to be considered amid the interconnect configuration forms, for example, wire estimating and repeater [70].

Gate and interconnect delay versus technology generation. However, this picture demonstrates that the interconnect challenges are even more severe for current and future technology nodes in Fig. 3.5

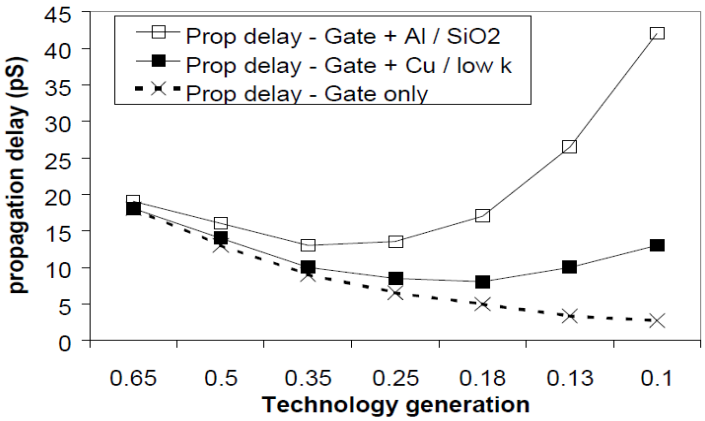


Figure 3.5: Interconnect delay V/s Technology generation [72].

One of the major reasons for the Interconnect to limit the performance of a circuit is the resistance-capacitance (RC) effect. As the chip area increases, parasitic interconnect capacitance dominates the gate capacitance and the speed improvement expected from simple scaling does not apply to circuits that drive global communication lines. Cu was an optimal material for interconnects in ICs throughout most of 20th century IC history, which was only natural following the great success of Cu wires in long-haul electricity networks. Be that as it may, as designers attempted to stay aware of the savage Moore's law, multiplying the quantity of transistors on ICs each couple of years, the interconnect measure needed to keep pace. The rising resistivity in turn leads to strong heating and increased power consumption of the IC. In fact, the shrinking interconnect is the most likely reason your smartphone heats up with intense use, and it is also why your battery is consumed so quickly. Researchers are of course investigating viable alternatives to Cu where in OI, CNTs, GNRs are emerging of them.

3.2 Interconnects Evolution:

The evolution the various types of the Interconnects is as summarized in Fig. 3.6. Cu is the most suitable material regarding electrical conductivity, but it was not used in large scale production as the conductive material in via until 1997. Before 1997, tungsten (vias) and Al (lines) were the dominant interconnection materials. Several challenges were present which limited Cu deposition, such as patterning difficulties and silicon contamination. Volatile Cu compounds were unknown and the technology at the time required such compounds for metal deposition.

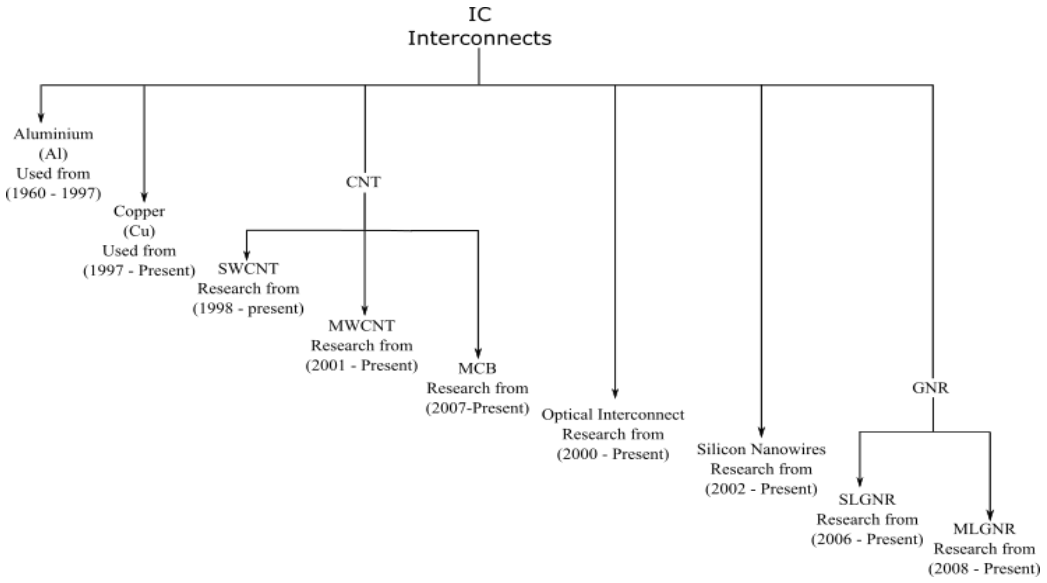


Figure 3.6: Evolution of interconnect [73].

There are two classes of developing interconnects: Cu substitutions, and local device interconnects. The Cu substitution alternatives supplant the Cu correspondence medium with different less develop advancements, including carbon-based and optical choices. The local device interconnect choices are exceptionally theoretical since they are by definition subordinate upon the utilization of new sorts of switches, however the thought of their properties is basic for driving the guide towards the right arrangements past the time allotment of the FET switch [105]. There are many challenges with implementation of Cu interconnects at the 32nm node and beyond, including increased resistivity, integration with porous low-k materials, and reliability [70, 74].

Table 3.1: Advantages and Concerns for Cu Extensions, Replacements and Native Device Interconnect ITRS-2011[23].

Emerging materials to replace Cu	**Potential Advantages**	**Primary Concerns**
Other metals (Ag, silicide, stacks)	Potential lower resistance in fine geometries	Grain boundary scattering, integration issues, reliability
Nanowires	Ballistic conduction in narrow lines	Quantum contact resistance, controlled placement, low density, substrate interactions
Carbon Nanotubes	Ballistic conduction in narrow lines, electromigration resistance	Quantum contact resistance, controlled placement, low density, chirality control, substrate interactions, parametric spread
Graphene Nanoribbons	Ballistic conduction in narrow films, planar growth, electromigration resistance	Quantum contact resistance, control of edges, deposition and stacking, substrate interactions
Topological Insulators	Suppression of elastic backscattering, spin polarized transport	No suppression of inelastic backscattering, inability to stack
Optical (interchip)	High bandwidth, low power and latency, noise immunity	Connection and alignment between die and package, optical /electrical conversion efficiencies
Optical (intrachip)	Latency and power reduction for long lines, high bandwidth with WDM	Benefits only for long lines, need compact components, integration issues, need WDM
Wireless	Available with current technology, parallel transport medium, high fan out capability	Very limited bandwidth, intra-die communication difficult, large area and power overhead
Superconductors	Zero resistance interconnect, high Q passives	Cryogenic cooling, frequency dependent resistance, defects, low critical current density, inductive noise and crosstalk

3.2.1 Interconnects and its Material:

A) Requirement of Interconnects:

- Low resistivity of conductors, low capacitance implies low dielectric constant.
- Low RC delay, Low cross talk, Low power dissipation (CV^2f loss).
- Resistance to electromigration.
- Ease of deposition of thin films of the material.
- Ability to withstand the chemicals and high temperatures required in the creation procedure.
- Ability to be thermally oxidized Good MOS properties.
- Good adhesion to other layers - low physical stress.
- Stability of electrical contacts to other layers.
- Ability to contact shallow intersections and give low resistance.
- Ability to be defined into fine patterns- dry etching.

B) Interconnect Material:

Copper (Cu):

Table 3.2: Merits and Demerits of Cu.

Merits	Demerits
▪ Cu is more conductive than Al, thus allowing finer metallization with lower resistive losses (ρ_{Cu} = 1.67 μΩ cm, ρ_{Al} = 1.65 μΩ cm) ▪ Atomic migration in Al occurs along grain boundaries and surfaces. There is little or no bulk transport in Cu. (Bulk self-diffusivity of Al: 1.9×10^{-12} m^2 s^{-1}, Cu: 1.8×10^{-16} m^2 s^{-1} at 933 K) ▪ Al is very susceptible to electro-migration, (get rapid formation of hillocks and voids), whilst Cu is less vulnerable as it has higher mass and a higher melting point. ▪ Cu is also less likely to fracture under stress.	▪ Cu diffuses rapidly into Si and SiO_2, causing deep-level defects as it contaminates the Si. ▪ The main transport path in Cu is the top surface of metallization lines. This results in some electromigration damage. Al-based metallization does not exhibit this, as Al forms a protective oxide layer preventing surface transport. ▪ As Cu cannot be dry etched, it was necessary to develop an electroplating process for making copper networks, the dual-damascene chemical-mechanical polishing (CMP) process, and an effective linear material for use as a copper diffusion barrier and to promote adhesion.

Because of the ideal properties of Cu, it is workable for the chip size to be decreased, while expanding the speed and multifaceted nature of the device. Cu has

turned out to be an astounding metallization material as it has an enhanced current conveying ability and high electromigration protection. It is in this manner feasible for part size to be additionally diminished, expanding the speed and many-sided quality of the device. This is adequate for the time being; however there is a proceeding with need to accomplish high conductivity and infinitesimal dielectric constants for future devices. In this way, all together for the microelectronics business to stay aware of Moore's Law and the regularly expanding shopper needs, there is a squeezing requirement for presentation of new materials and procedures.

Carbon Nanotube (CNT):

CNTs have novel nuclear plan and band structure that is in charge of their extraordinary electrical and mechanical properties [69]. These unprecedented properties make CNTs a standout amongst the most adored Interconnect materials in current nanoscale innovation. Some of these properties are quickly talked about underneath:

a) They can lead expansive current at littler cross-sectional region with no signal deterioration while all the while maintaining a strategic distance from electromigration issues that are generally common in metallic interconnects.
b) The resistance of the packaged CNT is around three requests of size lower than single CNT. Hence, it is normal that the CNT package would end up being successful substitution of Cu for interconnects as well as in future VLSI chips.
c) As the component measure decreases, the execution of Cu interconnects extremely degrades because of the expanded surface scattering in this way, radically diminishing the viable mean freeway. in any case, rather than Cu the CNTs supports ballistic flow of electrons with an electron mean free way of a few micrometers that unequivocally spur specialists to supplant Cu by CNTs.
d) SWNT brings about high contact resistance and characteristic impedance. Along these lines, a bundle of closely packed parallel CNTs are favored. The coveted properties of the nanotube bundle incorporates [69]:
    1) Low contact resistance with all nanotubes within a bundle.
    2) Distance between the nanotubes within the bundle should be as small as possible to have the large nanotube density.
    3) Quantum coupling between the nanotubes should be nearly zero.

CNTs are modest tubes around 10,000X more slender than human hair and comprise of moved up sheets of carbon hexagons. There are for the most part two sorts of CNTs that can have higher structural perfection. SWNTs comprise of single graphite sheet consistently wrapped into a round and hollow tube. MWNTs include a variety of such nanotubes that are concentrically settled like rings of a tree trunk. Electrical transport in metallic SWNTs and MWNTs is ballistic that outcomes in development of electrons without dispersing along the nanotube pivot. It empowers CNTs a long mean freeway in the scope of micrometer [69].

In realistic nanotube interconnects will be a mixed bundle of SWCNT and MWCNT. MCB is a combination of SWCNT with diameter (d) equal to1nm and MWCNT with multiple shells with various diameter‘d’ where (D_1 - D_n) as shown in Fig. 3.7. Contrastingly, the electrons in Cu can travel just 40–50 nm before disseminating. Strikingly, Plasmon's likewise engender effortlessly along the nanotube. Superconductivity has additionally been seen at low temperatures with change temperatures of about 0.55K for 1.4nm distances across SWNTs and almost 5K for 0.5nm SWNTs. The exceptional electrical properties of CNTs having to great degree low electrical protections are seen because of their novel electronic structure upheld by their 1D structure. Fundamentally, the protection is seen because of the defects in crystal structures, impurity atoms, or an atom vibrating about its position in the crystal [69]. Depending on the direction in which CNTs are rolled (chirality), they exhibit either metallic or semiconducting properties. The graphene sheet can be rolled in many possible ways such as Armchair, Zigzag as shown in Fig. 3.8.

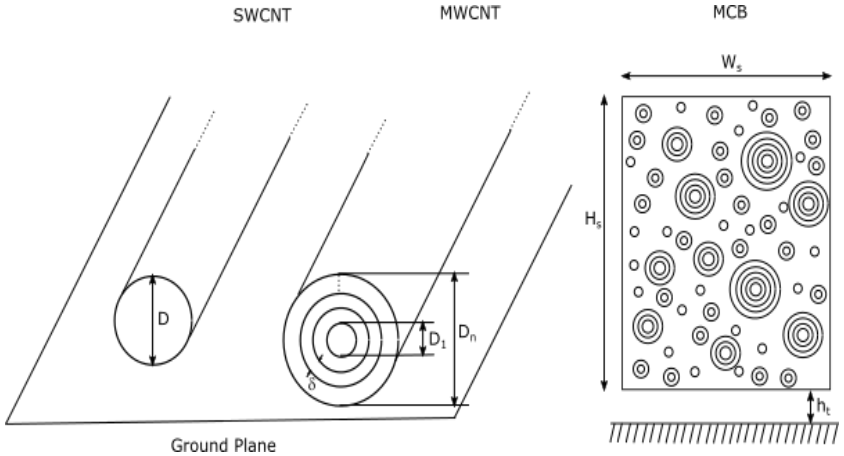


Figure 3.7: Single walled, Multi walled CNT and Mixed CNT Bundle [75].

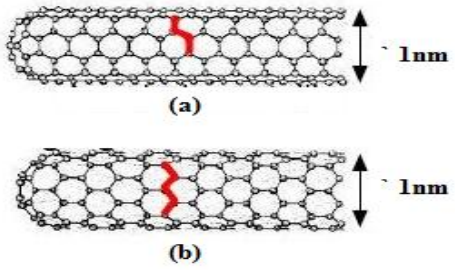


Figure 3.8: CNT types: (a) Armchair (b) Zig-Zag.

Because of littler distance across and higher perspective proportion, the electrons don't scatter much in CNTs that outcome in moderately bring down resistance than Cu. The low resistance guarantees that the vitality scattered in CNTs is inconceivably little. Consequently, the issue of scattered power thickness can be appropriately tended to that generally antagonistically influences the execution of silicon circuits. Current densities of more than 1010 A/cm^2 have been watched for the metallic CNTs [69].

The metallic CNTs are appealing interconnect materials due to their high warm and mechanical soundness, thermal conductivity as high as 5800W/mK, capacity to convey current in abundance of 1014A/m^2 current thickness even at temperatures higher than 200°C. It is exceptionally hard to make a good contact with a CNT. The unavoidable contact flaw builds protection. CNT protections in the range 7Kω-100Kω have been accounted for. Such a high resistance is a noteworthy detriment; if an isolated CNT is utilized as interconnect.

Advantages of CNTs:

CNTs offer several advantages compared to Cu/low-κ interconnects because of their one dimensional nature, the peculiar band-structure of graphene, and the strong covalent bonds among carbon atoms [23, 116]:

1. **Higher conductivity:** Due to their one-dimensional nature, the phase space for electron scattering in CNTs is limited, and electron mean free path is in the micron range for high quality nanotubes, in contrast to 40 nm in bulk copper. The conductivity of densely-packed CNTs is higher than scaled Cu interconnects for large lengths. Conductivity of short CNT bundles, however, is limited by their quantum resistance. Metallic SWCNTs have two conduction channels, and their quantum resistance is 6.5kΩ.

2. **Resistance to Electromigration:** The strong sp2 carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for CNTs; $10^9 A/cm^2$ in contrast to $10^6 A/cm^2$ in Cu. In practice, however, contacts may limit the maximum current density in CNT interconnects.
3. **Thermal conductivity:** The longitudinal thermal conductivity of an isolated CNT is expected to be very high, on the order of 6000W/mK, as suggested by theoretical models and extrapolations on measured data from porous bundles. The thermal conduction in CNTs is highly anisotropic, and the transverse conduction is orders of magnitude lower than the longitudinal conduction.

Graphene Nanoribbons (GNR):

Graphene is a one atom thick sheet of sp2-reinforced carbon atoms arranged in a honeycomb cross section structure, was as of late appeared to exist in a steady state in nature. It is a semiconductor with zero bandgap, phonon like 2D bound properties, linear energy dispersion, ambipolar charge transport, and a high carrier portability of $104 cm^2/Vs$ at room temperature. Control of the electrons of graphene in one of the in-plane ways is required and it brings about GNR. These strips will be segments of graphene with measurement under 10nm, purported GNR [76].

A few hypothetical examinations have been directed into exploring the electronic properties of graphene nanoribbons, for example, tight-binding calculations, and density functional theory (DFT) calculations. GNR can be of two sorts relying on their end style. Fig. 3.9 demonstrates the structures of Armchair and Zigzag GNRs. Width of armchair GNR is chosen by the quantity of hexagonal carbon rings or for the most part eluded as dimer lines (Na) over the ribbon. Likewise width of zig-zag GNR is subject to the quantity of zig-zag chains (Nz) over the ribbon.

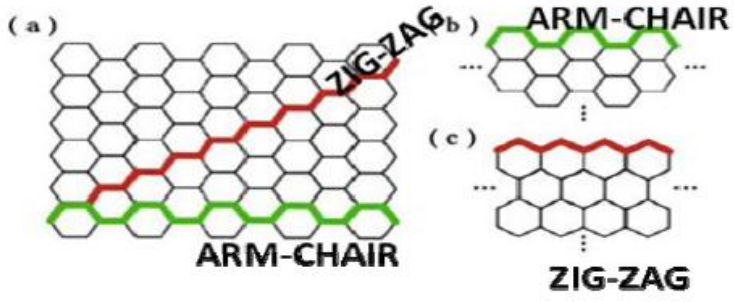


Figure 3.9: (a) Structure of GNR (b) Armchair, (c) Zig-Zag [76].

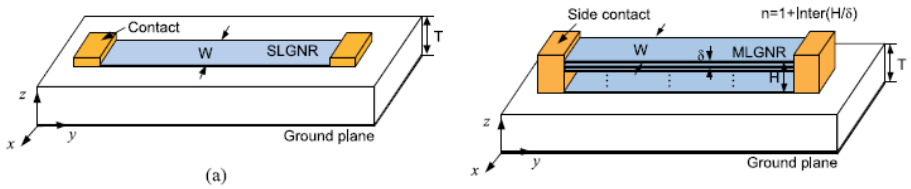


Figure 3.10: Single-layer GNR and Multilayer GNR structure [77].

The GNR interconnects can be named SLGNR and MLGNR relying on the quantity of layers as appeared in Fig. 3.10. SLGNRs have higher resistance so they don't fit for the interconnect applications however as MLGNRs have numerous parallel conduction ways so their resistance diminishes by the idea of parallel resistances and along these lines they are appropriate for the interconnect applications in sub-micron VLSI circuits [76]. High mean free path of electrons, smaller capacitance, and higher current carrying capacity make graphene an interesting candidate for replacing copper as the on-chip interconnect material.

Advantages of GNRS:

GNRs offer several advantages compared to Cu/low-κ interconnects [23, 116]:

1. **Higher conductivity:** Like carbon nanotubes, the mean free path of electrons in pure high-quality graphene can be quite large. Mean free paths as large as a few hundred nanometers have been reported in graphene. Substrate-induced disorders are believed to be the dominant source of electron scattering and high motilities corresponding to mean free paths as large as a few micrometers have been reported in the case of suspended graphene. Conductivity of stacks of non-interacting GNRs with smooth edges and Fermi energies above 0.2eV has been predicted to outperform those of copper wires, especially at small cross-sectional dimensions and long lengths.
2. **Resistance to electromigration:** The strong sp2 carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for GNRs; 10^9A/cm^2 in contrast to 10^6A/cm^2 in Cu. In practice, however, contacts may limit the maximum current density in GNR interconnects.
3. **Thermal conductivity:** The in-plane thermal conductivity of suspended single layer graphene sheets has been measured to be 5300W/mK. This value is comparable to the highest values reported for SWCNTs bundles.

A silicon nanowire has low conductivity compared to bulk material and Gold is used for nanowire growth which is rare earth material and hence cannot be used for bulk manufacturing process.

Table 3.3: Comparison of Cu, CNT and GNR [72].

Parameters	**Cu**	**CNT**		**GNR**	
		SWCNT	**MWCNT**	**SLGNR**	**MLGNR**
Max Current Density (A/cm^2)	10^7	$>10^9$	$>10^9$	$>10^8$	$>10^9$
Melting Point (k)	1356	3800 (graphite)			
Thermal Conductivity ($\times10^3$W/mk)	0.385	1.75-5.8	3	3-5	4-6
Temperature Coefficient of resistance ($\times10^{-3}$/k)	4	<1.1	-1.37	-1.47	-0.6
Mean Free Path (nm) @ room temperature	40	$>10^3$	2.5×10^4	1×10^3	$1\text{-}5\times10^3$
Bandwidth at 22nm global level (GHz) t=d=13.92	7.5MHz	54MHz	60MHz	3GHz	3.5GHz
PDP at 22nm (Global)	2.1pJ	6.24aJ	-	80.25aJ	-
Fabrication process	• Barrier Layer • Copper Seed Layer • Copper deposition	• Ta Layer • Ti Layer • Co Layer • CNTs (by PECVD)		• Ta Layer • Ti Layer • Co Layer • GNRs (by CVD)	

3.3 CMOS and Post CMOS Emerging Devices

The design of energy efficient FPGA Architecture of a system can be influenced at several design levels like the system, algorithm, data, circuit, device and the technology level.

3.3.1 MOSFET:

The MOSFET is the fundamental type of device in the standard complementary MOS (CMOS) technology. The working rule of a traditional long-channel MOSFET depends on drift-diffusion of charge carriers from the source to the

drain through injection into the channel. When a potential difference is created between the source and drain, the device is out of equilibrium and carriers can drift from the source to the drain, which result in a source-to-drain current Is=Id, if gate leakage Ig is neglected. The gate works as a switch: it controls the potential barrier height in the channel, and thus controls Id.

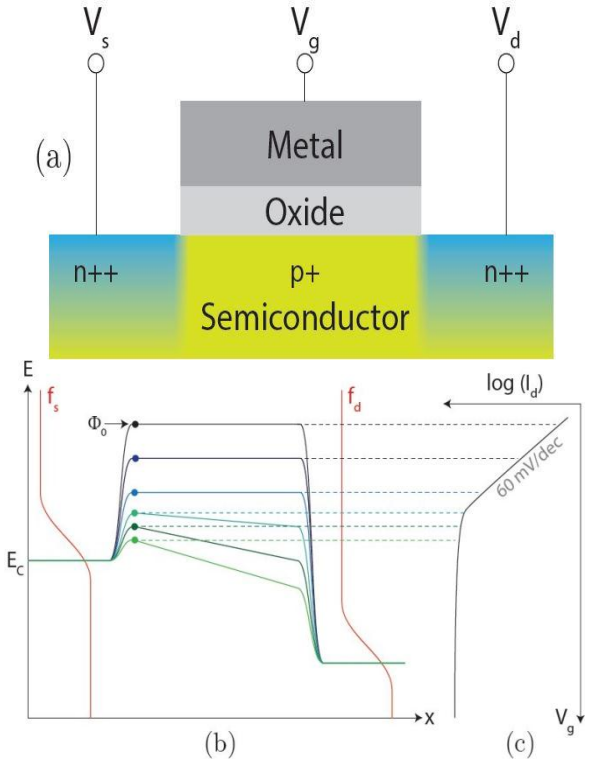


Figure 3.11: The working principle of a MOSFET.

(a) Cross section of an n-type device,

(b) Band structure (represented by the conduction band edge EC) of an n-MOSFET under positive '*Vds*' bias, '*fs*' and '*fd*' are the Fermi distribution in source and drain, individually. A positive '*Vgs*' will lower the channel barrier and increase the current from source to drain.

(c) Current '*Id*' is plotted logarithmically as a function of '*Vgs*'.

Limitations due to scaling of conventional MOSFETs

Various setbacks posed by scaling conventional MOSFETs are [78]:

a. Channel Length Modulation

At the point when the MOSFET is downsized to bring down measurements, modified channel abbreviates as drain bias is expanded consequently offering rise to channel length modulation which as a result builds drain current for a MOSFET which works in saturation and additionally decreases output resistance of

MOSFETs. The shortening of channel region occurs because of expansion of the non-inverted region towards source as drain voltage is made high. Henceforth lessening of output resistance occurs because of decrease in length thus causing an increased drain current.

b. Short Channel Effects (SCEs)

A semiconductor gadget is said to be a short channel gadget when its channel length ends up noticeably equivalent to drain depth and source depth and also depletion width. Major SCEs are explain as below.

a. Velocity Saturation of Carriers

At the point when the MOSFETs are downsized to low measurements, the charge carriers encounter extremely solid electric fields because of which their speed achieves a most extreme and saturates accordingly; there would be never again increment in carrier velocity when connected electric field is expanded further. This marvel gives impediment to carrier movement in semiconductor and is henceforth called speed immersion impact which is one of the major SCE.

b. Drain Induced Barrier Lowering (DIBL) and Punch Through

In small channel MOSFETs, at relatively high drain voltages, V_{th} lessens dissimilar to long channel devices where V_{th} is free of drain voltage. This wonder happens in short channel MOSFETs as drain voltage is extended, the depletion region of the drain-body junction stretches out under gate and hindrance bringing down of electrons in channel happens and limit voltages diminishes. Thus named as the impact as Drain Induced Barrier Lowering (DIBL).

c. Surface Scattering

In little channel estimations, vertical piece of electric field enliven electrons towards the surface which encounter crash and faces inconvenience as they go through the channel. This limits the adaptability of electrons and the wonder subsequently named surface diffusing.

d. Impact Ionization

Because of the nearness of extremely longitudinal electric field in short channel MOSFETs, electrons have higher speed, which impacts silicon atoms and ionize them which create electron hole combine. This wonder heightens when electrons due to high fields, go to substrate while trying to escape from the drain region and hereafter can impact the adjacent gadgets on the chip.

e. Hot-Carrier Injection

A component that can change the exchanging qualities for all time for a transistor, where an electron and also a hole can increase high active vitality and go into the dielectric of the MOSFET. This makes semiconductor gadgets less dependable.

f. Narrow Channel Effect

In little channel width gadgets, depletion region in the channel territory is greater appeared differently in relation to what is acknowledged. This happens due to bordering fields. From this time forward on account of thin channel, confine voltage of the gadget increases.

g. Subthreshold Conduction

Subthreshold conduction is the drain current among source and drain in the subthreshold region of MOSFET. Hence, consistent MOSFETs can't be looked upon as the gadget of future semiconductor world as it can be progressed to a particular most extreme in a manner of speaking. The subthreshold swings of standard MOSFETs have a base purpose of imprisonment of 60mV/decade. MOSFETs have I_{ON} to I_{OFF} extent in the demand of 103 to 104.

So the device engineers proceed with non-customary gadget with subthreshold swing under 60mV/decade and higher I_{ON} with uncommonly superfluous I_{OFF} attempting to impact them to go about as perfect switch.

3.3.2 Tunnel FET:

Scaling down of the MOSFET for the sake of reducing the power density resulted into reduction in the operating supply voltage as well. Tunnel Transistor has been evolved in 1992 by T. Baba, as one of the promising alternatives to the conventional MOSFET [79] based on various performance parameters as mentioned belows:

- Potential for exceeding the 60mV/decade sub-threshold swing.
- Ultra-low power and ultra-low voltage, Short Channel Effects.
- Reduction in the leakage currents, Higher I_{OFF}/I_{ON} current ratio.
- Exceeding the Speed requirements due to tunneling effects.
- Ability to take a shot at sub-threshold and super-threshold voltage.
- Similarity in manufacture process as contrasted and MOSFET [79].

Taking into consideration the above parameters, the MOSFET could be replaced by a potential substitute in terms of TFET for the purpose of ultra-low power, high speed and energy efficient applications in the domain of IC [80]. The scaling of the MOSFET has diverse bottlenecks the extent that its ability to work in ultra-low power, leakage currents, SCE, speed upgrades and so forth had prompted constraint of the execution of MOSFET. Keeping up set up the electric fields while cutting back the MOSFET the channel length and oxide thickness are scaled by 1/K while the substrate doping is scaled up by K, where K is a scalar steady. This kind of scaling is known as R. Dennard scaling [81]. For exhibit day contraptions, R. Dennard scaling doesn't fill in as it used to be already. The reason can be cleared up using Fig. 3.12 which shows the assortment in V_{DD} and V_T.

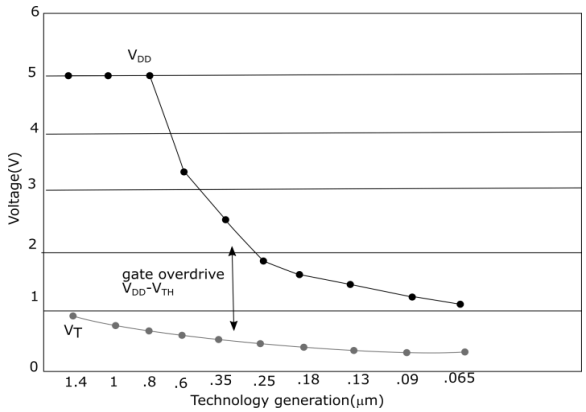


Figure 3.12: Plot of technology generation V/s $V_{DD,}$ V_T voltage [81].

A) Design Parameters:

The most basic aftereffect of scaling is that the gate overdrive voltage (V_{GS} - V_T equivalent to V_{DD}-V_T) remains for all intents and purposes reliable for front line development center points (short channel lengths). At the point when gate overdrive voltage diminishes, at that point on-current declines which adversely influence device execution, for example, I_{ON}/I_{OFF} proportion and dynamic speed (CVDD/I_{ON}). There are two conceivable answers for this issue of low I_{ON} of cutting edge innovation hubs, (a) Increase V_{DD} (b) Reduce V_T [81].

a) Increasing V_{DD}

For an inverter, the dynamic power consumption can be expressed in

$$P_{dynamic} = f\, C_L\, V_{DD}^2 \quad \text{..... (3.2)}$$

Where 'f' is the frequency of operation and 'C_L' is the capacitive load.

As can be seen, with increase in V_{DD} the dynamic misfortune in the gate inverter increases. Basically, the static power use is given by

$$P_{leakage} = I_{leak}\ V_{DD} \quad \text{.....(3.3)}$$

Where 'I_{leak}' is switch off leakage current of MOSFET in the device structure. It is clear from the above expressions that both static and dynamic power loss of the devices increases as a function of supply voltage (V_{DD}).

b) Reducing V_T

Second option for keeping the high gate overdrive is to scale down V_T. For an average 60mV/decade reduction in V_T, the I_{OFF} or sub-threshold current increase by 10X of its initial value which results in increase in leakage power. Presently when innovation downsizes up to nanometers, transistors tally per unit chip territory increments along these lines its leakage power requirements likewise increments. Because of this its standby power utilization in the device likewise increments. The lessening in the V_T is not the best possible arrangement from the above discourse [82].

In order to solve these issues, recent literatures have proposed TFETs. The advantages of TFET are low sub-threshold current which leads to low leakage per device and its high I_{ON}/I_{OFF} ratio can be suitable for memory application, etc. As discussed above there are limitations with V_{DD} and V_T scaling. Fig. 3.13 addresses the movements of leakage energy (EL) and dynamic energy (EDYN) with supply voltage V_{DD} for both MOSFET and TFET [83].

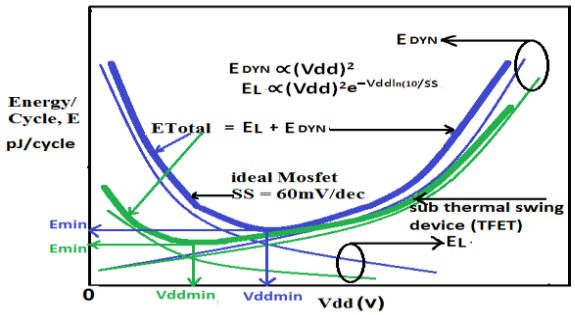


Figure 3.13: Plot of E_{DYN} and E_L V/s Supply voltage V_{DD}: Energy dissipation is lower for lower SS devices (TFET) [84].

The expression for (E_{DYN}) and (E_L) are as given below [83]:

$$E_{DYN}\ \alpha V_{DD}^2 \quad \text{.....(3.4)}$$

$$E_L / V_{DD}^2\ 10(-V_{DD}/SS) \quad \text{..... (3.5)}$$

Equations 3.4 and 3.5 states that for MOSFETs, both the leakage and dynamic energy are proportional to V^2_{DD}. However, leakage energy also has an additional exponential dependence on SS.

As specified some time recently, evolving V_{DD}, influences the device execution. Hence, one path is to discover a device with bring down sub-threshold swing (SS < 60mV/dec). TFET displays these attributes. Consequently, at bring down voltages (V_{DD}), TFET displays bring down ET (Total energy=EL+EDYN) contrasted with a MOSFET [82]. The TFET follows band-to-band tunneling mechanism with the quantum-mechanical generation of carriers. Scaling of a gate length in the MOSFET, it shows short channel effects for a span of higher number of the electron wave-length. The TFET is highly compatible for standard CMOS process flow. Therefore, TFET is an emerging alternative type for next scaling of the gate length however which is not affected by SCEs. As the device structure of TFET is decreases its static power consumption gets reduced ultimately [84, 85]. In the ON province of TFET, the bearers burrow through the obstruction which is band gap between valence band and conduction band for the stream of current from drain to source. Whereas in OFF state, available barrier maintains I_{OFF} magnitude lower than that of I_{OFF} magnitude of the conventional MOSFET. These properties make TFETs suitable for low power digital applications [82].

B) TFET Device Physics and Operation:

a) Band to Band Tunneling

The Band to Band Tunneling (BTBT) wonder gives a verbalization to the tunneling transmission of carriers and can be fulfill by Wentzel, Kramer's and Brillouin (WKB) figure and considering the passage obstruction as a triangular shaped potential impediment. According to WKB approximation,

$$T_t \approx \exp\left[-\frac{4}{3}\frac{\sqrt{2m\cdot}}{qF\hbar}.\left(E_g\right)^{3/2}\right] \quad \text{.....(3.6)}$$

Equation (3.6) is a general articulation for band-to-band tunneling transmission. Where k(x) is the quantum wave vector of the electron inside the triangular barrier,'m' is the electron powerful mass, '$\hbar$' is Planck's constant divided by 2 2π, '*Eg*' is the band gap of the semiconductor material at the tunnel junction, and '*F*' is the electric field measured in V/m. There are four important conditions in order for band-to-band tunneling to take place:

1. Available states to tunnel-from,
2. Available states to tunnel-to,
3. An energy barrier that is sufficiently narrow for tunneling to take place and
4. Conservation of momentum.

b) Subthreshold swing in Tunnel FETs

In order to describe the expression for the sub-threshold swing of a band-to-band tunneling device, consider the band to band Tunneling current is given below [84] for reverse-biased p-n junction:

$$I = aV_{eff}E_e^{\frac{-b}{E}} \quad \text{..... (3.7)}$$

Where,

$$a = Aq^3\frac{\sqrt{\frac{2m\cdot}{E_g}}}{\hbar^2\pi^2} \quad \text{..... (3.8)}$$

Where '*A*' is the device cross sectional area and

$$b = 4\sqrt{m\cdot}\frac{{E_g}^{3/2}}{3q\hbar} \quad \text{.....(3.9)}$$

Accordingly, the sub-threshold swing in a TFET increases with gate-source voltage and much steeper at lower gate voltages. The second term describes that the derivative of the junction electric field on the gate-source voltage should be maximized [82].

Different Structures of TFET:

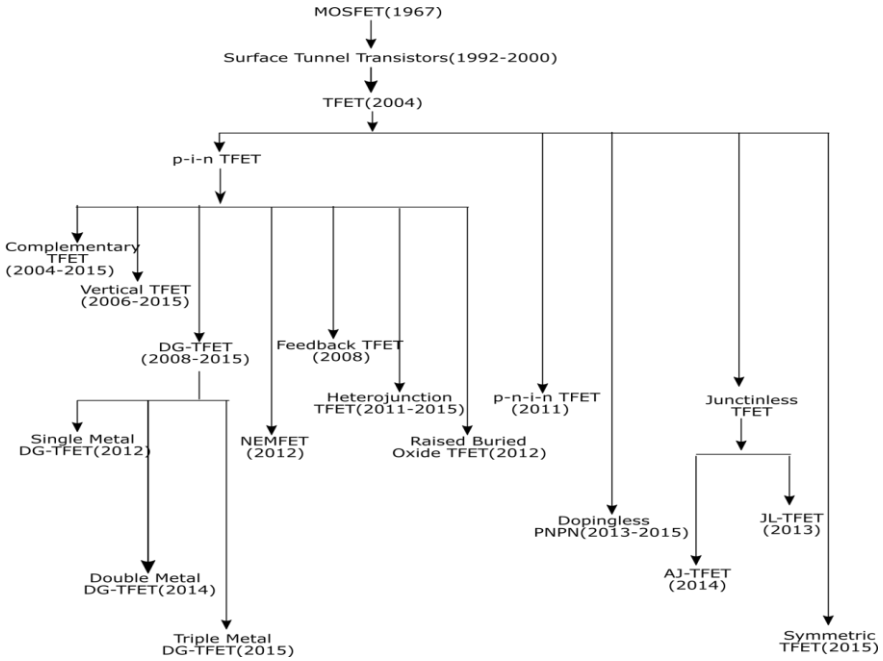


Figure 3.14: Evaluation of TFET [87].

a) Surface Tunnel Transistors (1992-2000):

Toshio Baba presents a new type of tunnel device called the surface tunnel transistor (STT) which can operate normally even in very small structures with gate lengths of less than 0.1µm at room temperature. The STT consists of an $n^+/i/p^+$ diode structure with an insulated gate in the i-region. The drain must be highly degenerated and must make a tunnel junction with the 2D electron channel under the gate. The STTs were fabricated using a GaAs/AlGaAs heterojunction in order to study the basic characteristics of this new device. Their current-voltage characteristics exhibit transistor action without saturation characteristics in the drain current similar to a vacuum triode operation. These characteristics of STTs were anticipated by the theory of interband tunneling [88].

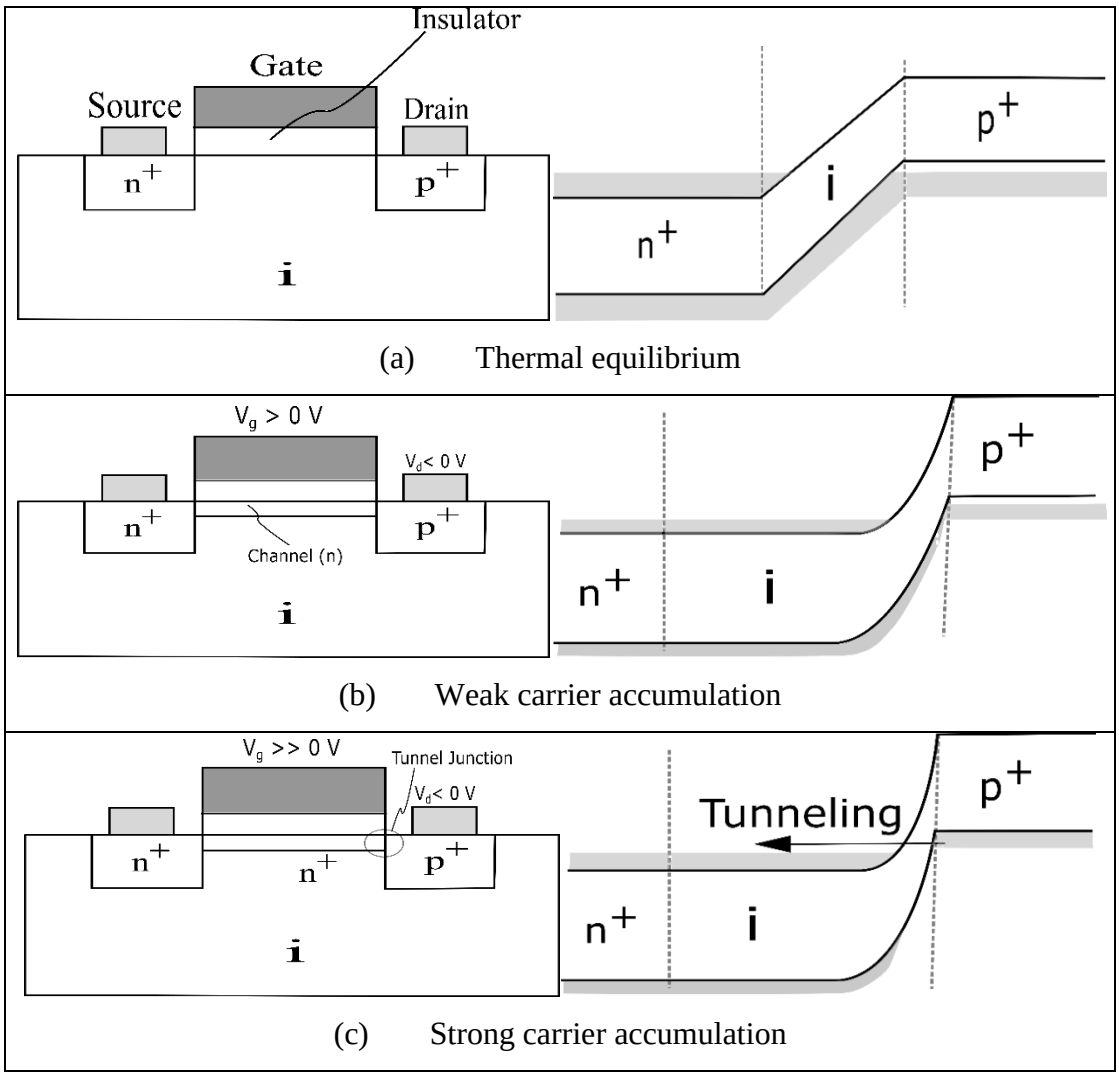


Figure 3.15: Schematic cross section of STT and band diagram at semiconductor surfaces [88].

Fig. 3.15 a-c shows cross sectional view of the proposed STTs which consists of a drain, a source and an insulated gate. Although the STT structure is match to Si-MOSFET or HEMT, the doping polarity of the drain terminal is different from the source terminal. This is an important difference from conventional FETs. Moreover, the drain region must be highly degenerated and must also have a very sharp doping profile for a low doped substrate. These are crucial factors for STT operation [88].

b) Single Metal Double Gate-TFET (2013-2015):

In an incorporated DG-TFET process, the TFET will profit by the additional gate, with the end goal that the current will be at least doubled. Thusly, the I_{ON} is helped, while the I_{OFF}, still in the fempto amperes or pico amperes run, increases by some factor yet stays to an extraordinary degree low [89].

The looked into DG-TFET gadget structure is a sidelong n-sort TFET in a thin Si layer, disengaged from the substrate by a dielectric layer. The basic framework is a gated p-i-n diode. The tunneling occurs in this gadget between the trademark and p+ regions [89]. Schematics of two of the gadgets reenacted are showed up in Fig. 3.16. To work these gadgets, the source is grounded, a low voltage (~0.1V) is associated with the drain, and a voltage is associated with the gate(s). Without a gate voltage, the width of the energy barrier between the intrinsic region and the p+ region is more extensive than 10nm (the surmised least to tunnel current to happen) and the gadget is in the off-state.

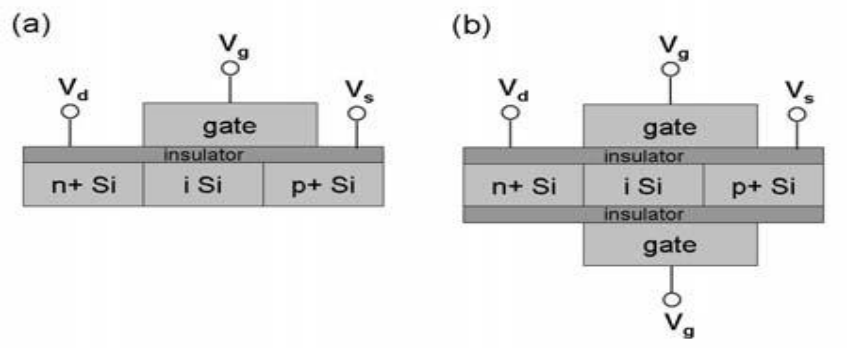


Figure 3.16: Simulated TFETs: (a) Single Gate (b) Double Gate [89].

The explored TFET indicates enhanced qualities, including higher on-current, bring down off current, and a lower subthreshold swing, after the proposed outline adjustments: a twofold gate, high-K gate dielectric, and upgraded Si body thickness. The twofold gate and high-K dielectric raise on-current to 1mA at Vg=1.2V, and give a comparing change in the normal subthreshold swing, as low as 52mV/dec and a

base point slant of 18mV/dec. An ideal silicon body layer thickness extending in the vicinity of 5 and 10nm is found for the considered gadget measurements, augmenting the proportion I_{ON}/I_{OFF} to 1013.

c) Single Gate Heterojunction TFET (2013-2015):

On account of Si TFETs the I_{ON} is low. It is a direct result of poor BTBT effectiveness. This issue can be abstained from utilizing Heterojunction materials, high-k gate insulators. The device is composed with the source material supplanted by SiGe material. The device goes for giving high I_{ON} without bargaining the I_{OFF} and SS [90]. Because of this I_{ON} is expanded because of decreased passage hole in ON state and I_{OFF} is diminished because of expanded passage hole in OFF state.

These devices have the gate set over the source. The tunneling in these TFETs happens consistently along the gate length and tunneling will be orthogonal to the door, hence enhancing the I_{ON} and the SS of the device.

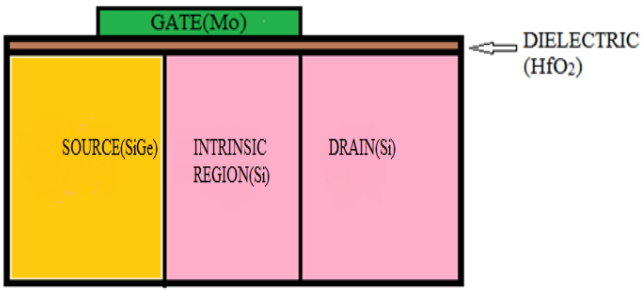


Figure 3.17: Structure of a line TFET with SiGe source [90].

The structure comprises of Si as drain, natural Si as channel, HfO_2 as gate oxide and molybdenum as gate. For N type, source is doped with P-type material and here Boron is utilized, intrinsic region and drain are dropped with N-sort material and here arsenic is utilized. The source doping is $1019cm^3$ intrinsic region doping is $1017cm^3$ and deplete doping is $1020cm^3$.

Table 3.4: Design parameters of the proposed device [90].

Sr. No	Parameters	Dimensions
1	Gate Length (Lg)	60 nm
2	Thickness of Gate Oxide (HfO_2)	1 nm
3	Doping Concentration for Source (SiGe)	1e+19
4	Doping Concentration for Intrinsic Region (Si)	1e+17
5	Doping Concentration for Drain (Si)	1e+20
6	Length of Channel	40nm
7	Channel Thickness Si	50nm

The device is worked by applying gate inclination so electrons are amassed in the intrinsic region. At the point when adequate gate bias is connected, band-to-band tunneling happens. As the gate bias inclination is diminished, the groups move toward becoming misaligned and current can never again stream. Generally, the band gap between the valence band of source and conduction band of intrinsic region are close to each other in TFET than conventional MOSFET [91]. At the point when SiGe is utilized the tunneling barrier is decreased and henceforth more electrons can burrow through the burrowing hindrance which thus builds the I_{ON}. The proposed gadget has higher I_{ON} of around 2.5mA/μm at a similar voltage conditions.

d) Single Gate PNPN TFET (2011 -2015):-

The silicon device innovation faces issue when devices downsize to nanometer measurements. Many difficulties happen, for example, SCEs like DIBN, lessened I_{ON}/I_{OFF} proportion, which may restrain the operation. Because of huge tunnelling width of the p-i-n structures, there is a voltage drop over the tunnelling intersection which brings about corrupted I_{ON} [92]. In general TFET on current is of the demand of 10μA which is two solicitations lower than 2009 ITRS essential. Conventional TFET is a gated p-i-n structure. A promising contender which does not encounter the evil impacts of these requirements is the Tunnel Source PNPN hetero junction TFET [93]. The possibility of PNPN TFET was proposed as a choice course of action towards fulfilling steep subthreshold conduct.

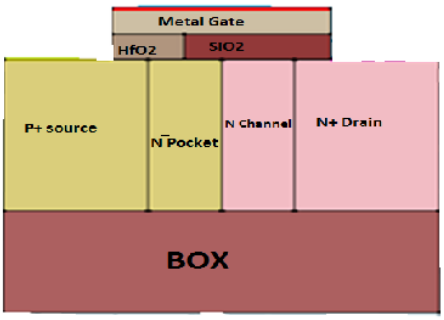


Figure 3.18: Device structure of PNPN TFET BOX with buried oxide [93].

PNPN TFET is a semiconductor device in which the gate controls the source to channel tunnelling current through modulation of BTBT. As opposed to using p+ source as in a customary TFET, a tunnelling junction is moulded between the p+ area and a completely exhausted thin n layer under the gate which diminishes the

tunnelling width and makes neighbourhood band bowing and in this manner steep SS. This n pocket improves the tunnelling finishing steep subthreshold lead and meanwhile gives high I_{ON} when appeared differently in relation to TFET.

This gadget is free from drifting body effect i.e the kink effect. Exactly when the drain voltage is adequately high, the channel electrons can secure satisfactory energy in the high electric field zone near the drain to influence electron to gap sets, in light of an impact ionization component. A low band gap material (Ge) is utilized as a part of source and pocket i.e. at the chose territory where BTBT will happen. This will build the tunnelling likelihood as tunnelling likelihood is a component of band gap Eg. The tunnelling likelihood is computed by Wentzel-Kramers-Brillouin (WKB) technique. High-K gate separator is somewhat situated at the source-channel intersection incites a neighbourhood least of the conduction band edge and low K gate cover at the drain end to lessen the extreme ambipolar current.

Table 3.5: Comparison Results [92].

L_g (nm)	**PNPN TFET**			**Conventional TFET**		
	R_{ON} (KΩ/μm)	**SS (mV/dec)**	**I_{ON}/I_{OFF}**	**R_{ON} (KΩ/μm)**	**SS (mV/dec)**	**I_{ON}/I_{OFF}**
30	42.6	53.1	10^8	64.1	93.2	10^5
35	46.1	55.3	4×10^7	61.2	90	10^5
40	48	62	6×10^7	60	91.2	0.1×10^6
45	48.5	65.6	4.2×10^7	58.6	91	0.2×10^6
50	50.2	68	10^7	57	90	0.4×10^6
55	53.3	72.2	0.6×10^7	53.8	72	0.7×10^6
60	62	73.2	10^6	50	71.3	10^6

PNPN heterogate SOI TFET has low SS and higher I_{ON}/I_{OFF} and, low R_{ON} when contrasted with traditional TFET. DIBN impact and wrinkle impact can likewise be wiped out because of FD SOI structure. Thus PNPN heterogate SOI TFET is appropriate for low power applications.

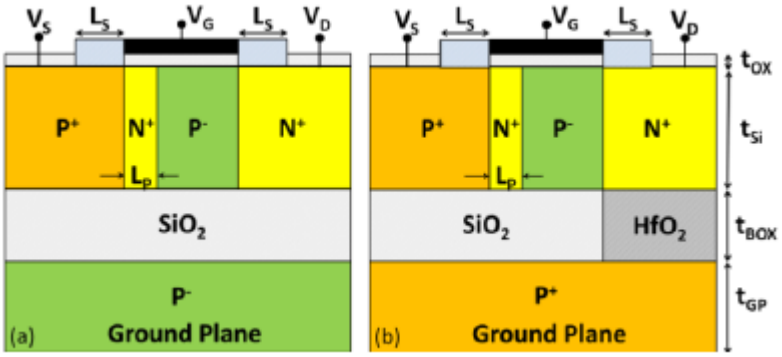


Figure 3.19: Schematic View: (a) Conventional PNPN TFET

(b) HBD PNPN TFET [92].

A hetero-dielectric BOX over an exceptionally doped ground plane can control the tunnelling width at the channel drain interface and incite an imperative diminishment in the ambipolar current in TFETs. The hetero-dielectric BOX comprises of SiO2 under the source and the channel districts, and HfO2 under the drain locale. Difference between general PNPN TFET and this gadget structure is, a hetero-dielectric BOX in which the high-k dielectric is set just underneath the drain and an energetically P+ doped ground plane is used instead of a delicately doped ground plane.

Table 3.6: Parameters used for device simulations [92].

Sr. No	Parameters	TFET	
		PNPN TFET	HBD PNPN TFET
1	Box Thickness (tBOX)	25nm	25nm – 40 nm
2	Ground Plane Doping (N_A)	1 x $10^{17}cm^{-3}$	1 x $10^{20}cm^{-3}$
3	SOI Film Thickness (t_{si})	10 nm	10nm
4	Gate Oxide (SiO_2) Thickness (t_{OX})	1nm	1nm
5	Gate Work Function	4.33eV	4.33eV
6	Gate Length	50nm	50 nm
7	Source Doping (N_A)	1 x $10^{20}cm^{-3}$	1 x $10^{20}cm^{-3}$
8	Drain Doping (N_D)	5 x $10^{18}cm^{-3}$	5 x $10^{18}cm^{-3}$
9	Channel Doping (N_A)	1 x $10^{17}cm^{-3}$	1 x $10^{17}cm^{-3}$
10	Source-Pocket Length (L_P)	4nm	4nm
11	Source-Pocket Doping (N_D)	1 x $10^{19}cm^{-3}$	1 x $10^{19}cm^{-3}$
12	Spacer between Gate and Source/Drain Contacts (L_s)	30nm	30nm

The proposed HDB PNPN TFET could be an attractive alternative to the conventional PNPN TFETs even for digital circuit applications.

3.4 Summary

A detailed survey of interconnects used in IC is presented here. From the inception of ICs Al was the first choice of material until the Cu was introduced. During each technology generation feature size of device and interconnect got reduced. Traditional on-chip metallic interconnects are beginning to show their limitations due to a number of reasons: high resistivity (due to electron grain and grain boundary scatterings, leading to large propagation delays, and poor performance), low reliability, and high susceptibility to electro-migration (at high current densities) with technology and interconnect scaling.

This chapter revealed that CNT, OI, GNR and SN, as conceivable substitution of ordinary Al or Cu based interconnects. As the technology node shrinks from 80nm to 14nm (and below), the electrical properties of ballistic conduction, ability to handle high current densities up to 10^{10}A/cm2 and high thermal conductivity make CNTs and GNRs far superior to Cu. MWCNT and MLGNR are better choice for on-chip interconnects. MCB is also applicable for global VLSI interconnects.

The next chapter deals with the performance evaluation of the conventional and developing devices.

Chapter 4

PERFORMANCE EVALUATION OF EMERGING DEVICES

Scaling of regular CMOS might be troublesome perhaps past 22nm innovation hub because of uncontrollable short-channel impacts and unreasonable V_{th} variety. Thus the novel transistor structures have been explored to support kept scaling. Henceforth, to extend their usage in ULP versatile space, there is a need to investigate the unwavering quality of these devices within the sight of PVT varieties under subthreshold conditions. In this way, this section investigates the execution of these devices for subthreshold circuits. The initial segment of this section manages essential properties of these devices alongside their qualities under subthreshold conditions. The second part at that point researches the impact of PVT minor departure from the execution of these gadgets.

4.1 Introduction

It is anticipated that CMOS innovation will likely go into 10nm hubs around 2018 according to Moore's Law. Scaling of CMOS innovation underneath 22nm innovation hub needs some critical changes in the innovation. Si-MOSFET shows huge postpone punishment at the cost of vitality sparing under subthreshold conditions. Additionally, subthreshold circuit qualities are touchier to PVT varieties. To manage these issues, there is a need to research the execution of MOSFET and TFET gadgets under subthreshold conditions in order to use their fast qualities notwithstanding for ULP applications. Henceforth, it is vital to investigate the capability of up and coming gadgets like TFET.

4.2 Device Simulations:

Considering importance of energy efficient FPGA research and possible realization of different device types in ultra-low power circuits, literature review of CMOS and Post CMOS Device types and the Interconnects for the performance analysis of FPGA circuits are presented in this report. Uniting the latest parallel computation development, the Genius Device Simulator can manage broad issues with no less than 200,000 work center points and is fit for quickening amusement times by a factor of at least 10 or more and is capable for circuit simulation and mixed device/circuit simulation.

At a startup stage, simulation of the conventional MOSFET and the variants of TFET based on Si, Ge, and SiGe is taken into consideration. This section explores the results and made the comparison of the same.

4.2.1 Device Simulation of CMOS – TFET

A) Simulation Results of MOSFET

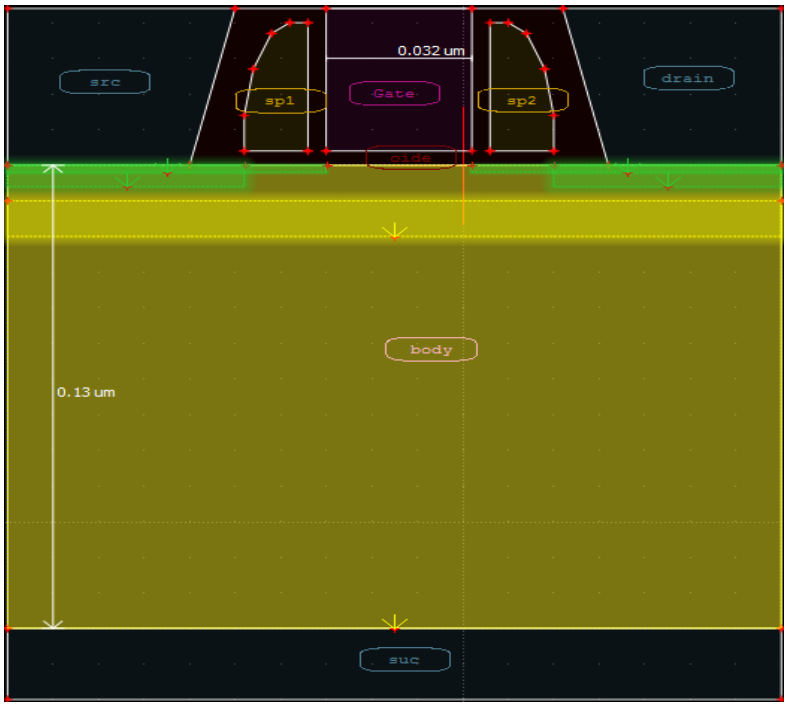
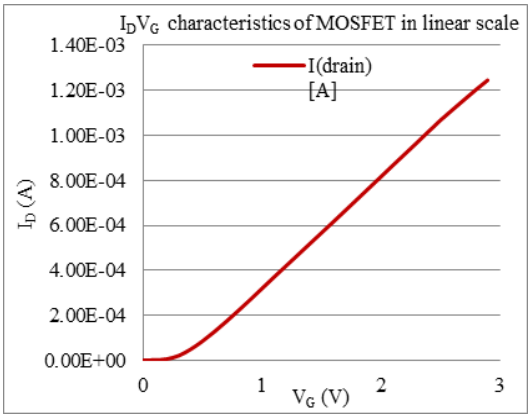


Figure 4.1: Device structure of MOSFET in TCAD.

Table 4.1: Parameter & values of MOSFET used in TCAD simulation.

Sr. No.	Parameter	Length	Material Used	Doping / Mesh Size
1	Gate	32nm	nPolySi	Mesh size= 0.003µm
2	Source	40nm	Al Lower Source Doping-	5e+20 (Y=0.001) 1e+18 (Donor)
3	Drain	40nm	Al Lower Drain Doping-	5e+20 (Y=0.003) 1e+18 (Donor)
4	Body	130nm	Si	Mesh size= 0.005 µm 5e+15 (Acceptor)
5	Oxide	4nm	SiO_2	Mesh size= 0.004µm
6	Substrate	20nm	Al	Mesh size= 0.004µm
7	Spacer1 & Spacer2	18nm	Nitride	Mesh size= 0.004µm
8	Inversion Layer	10nm	--	1e+18 (Acceptor) (Y=0.003)



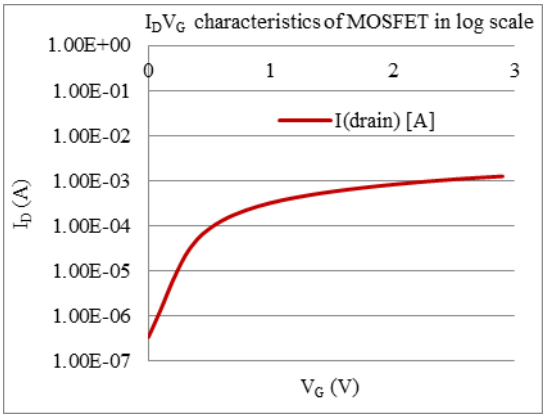


Figure 4.2: I_d-V_g characteristics of MOSFET using Si as body in linear and log Scale.

For the trial information of the NMOS with gate of 32nm, 5E+15cm^{-3} doped channel, the leakage current increments exponentially with the drain voltage. Similar changes are found in the simulated I-V characteristics of this transistor.

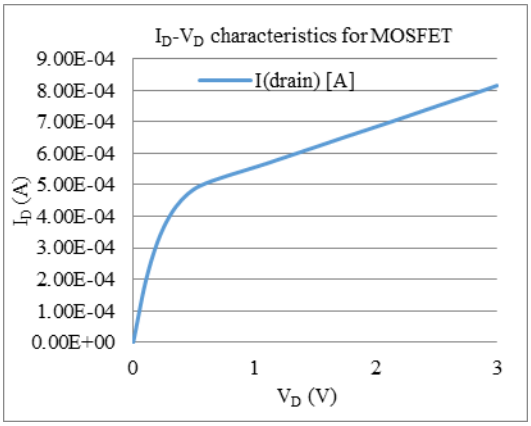


Figure 4.3: Id-Vd characteristics of MOSFET using Si as body.

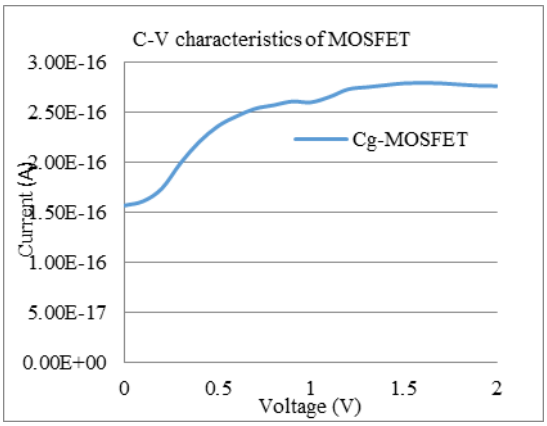


Figure 4.4: C-V characteristics of MOSFET.

It shows that as voltage increases capacitance of MOSFET is also increases.

B) Simulation Results of TFET (Ge, Si, SiGe)

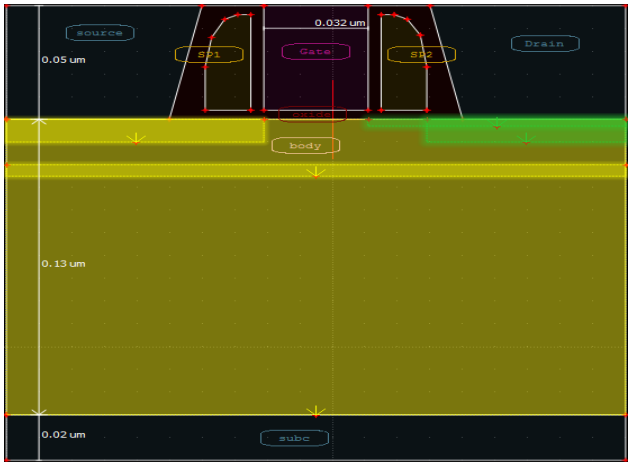
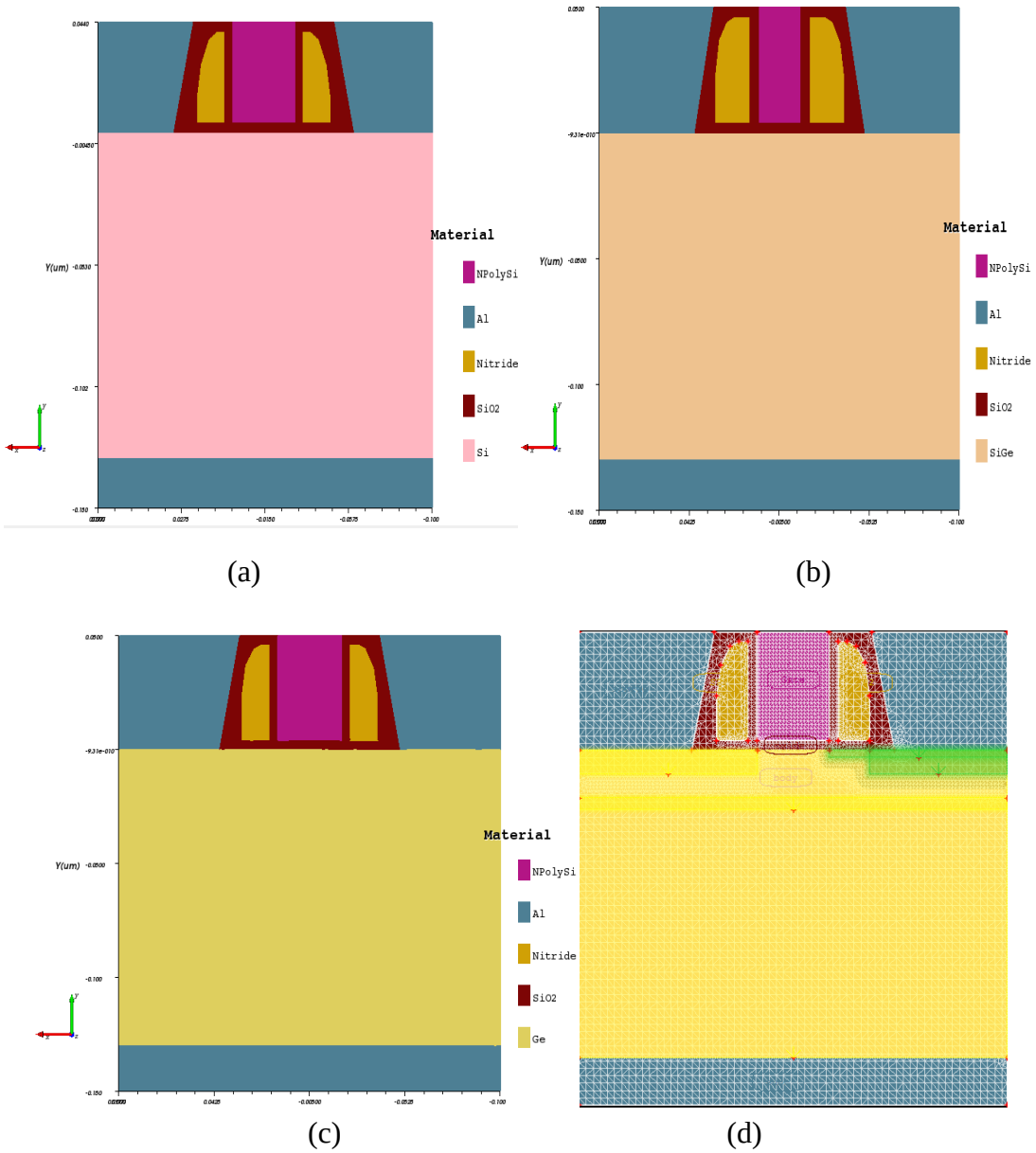


Figure 4.5: Device structure of TFET in TCAD.

Table 4.2: Parameter & values of TFET used in TCAD simulation.

Sr. No.	Parameter	Length	Material Used	Doping / Mesh Size
1	Gate	32nm	nPolySi	Mesh size= 0.003µm
2	Source	50nm	Al	1e+20 (Y=0.002) (Acceptor)
3	Drain	50nm	Al Lower Drain Doping-	1e+19 (Y=0.003) 1e+18 (Donor)
4	Body	130nm	SiGe	Mesh size= 0.005 µm 1e+17 (Acceptor)
5	Oxide	4nm	SiO_2	Mesh size= 0.004µm
6	Substrate	20nm	Al	Mesh size= 0.004µm
7	Spacer1 & Spacer2		Nitride	Mesh size= 0.004µm



(a) (b)

(c) (d)

Figure 4.6: Device meshing and materials of TFET: (a) Si TFET (b) Ge TFET (c) SiGe TFET (d) Meshing of TFET.

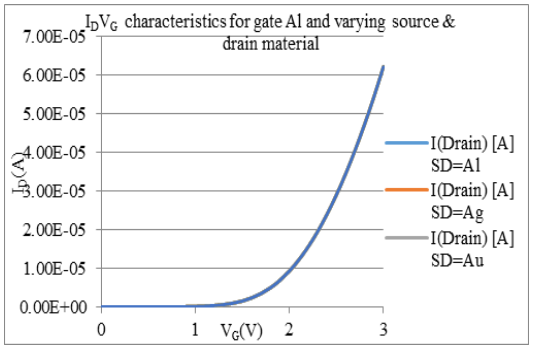


Figure 4.7: Id-Vg characteristics for gate Al and varying source & drain material.

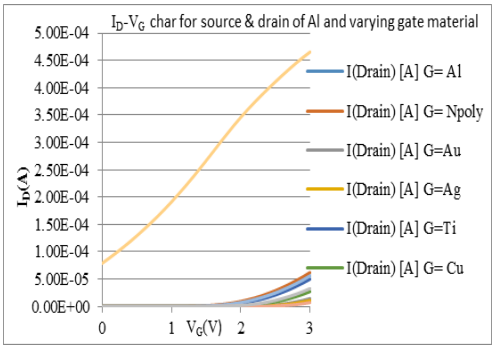


Figure 4.8: Id-Vg characteristics for source & drain of Al and varying gate material.

Material properties have various effects on device characteristics. Drain, source and gate metal contact material should be a good conductor. Gate material has very significant effect on drain current which controls the conduction channel, so gate material is varied keeping drain & source as Al as varying drain and source doesn't affect the characteristics as shown in Fig. 4.8. Various gate materials are used as Al, Npoly, Au, Ag, Ti, Cu, Elec, Ppoly, Pt, $TiSi_2$ out of which Npoly gives better results among other materials. Id-Vg characteristics for 0V<Vds<2V of the 32nm Npoly gate and Si body TFET are plotted on linear and logarithmic scale in Fig. 4.9. For Si TFET for Vds=1.2V, $I_{OFF}=2.5589e^{-13}$µA/µm at Vgs=0Vand $I_{ON}=4.6813e^{-05}$µA/µm at Vgs=3V. Id-Vg characteristics for 0V<Vds<2V of the 32nm Npoly gate and Ge body TFET are plotted on linear and logarithmic scale in Fig. 4.10. For higher gate voltage current gets saturated due to saturation of tunneling channel. For Ge TFET for $V_{ds}=1.2V$, $I_{OFF}=4.5221e^{-11}$µA/µm at Vgs=0V and $I_{ON}=9.7372e^{-05}$µA/µm at Vgs=3V.

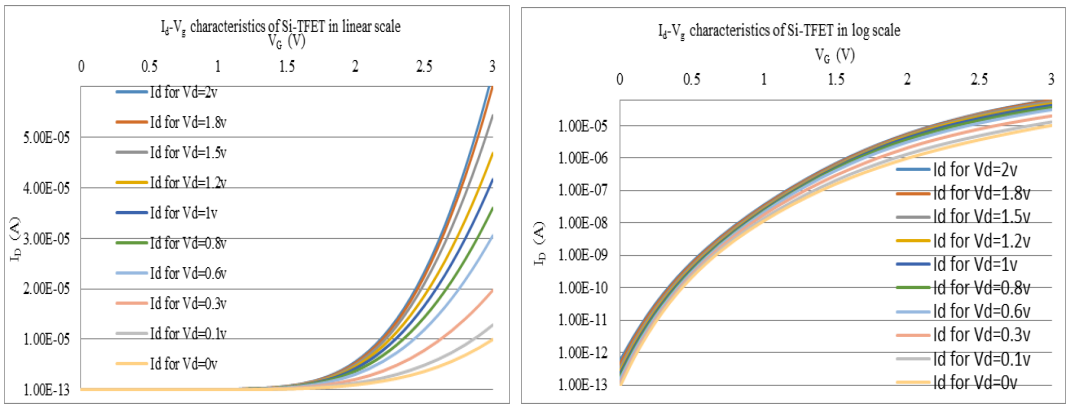


Figure 4.9: I_d-V_g characteristics of TFET using Si as body for various Vds in linear and log Scale.

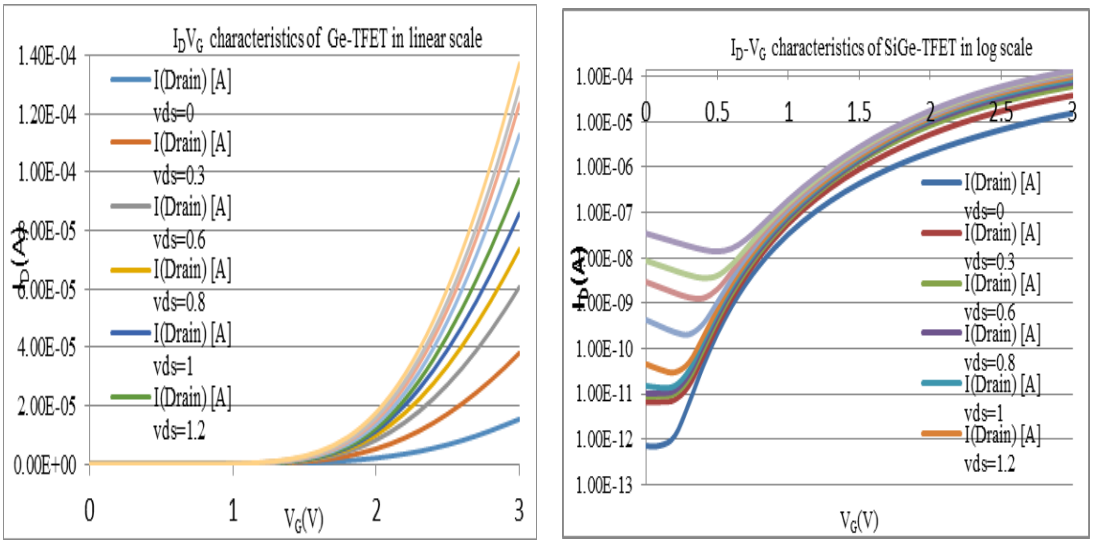


Figure 4.10: I_d-V_g characteristics of TFET using Ge as body for various Vds in linear and log Scale.

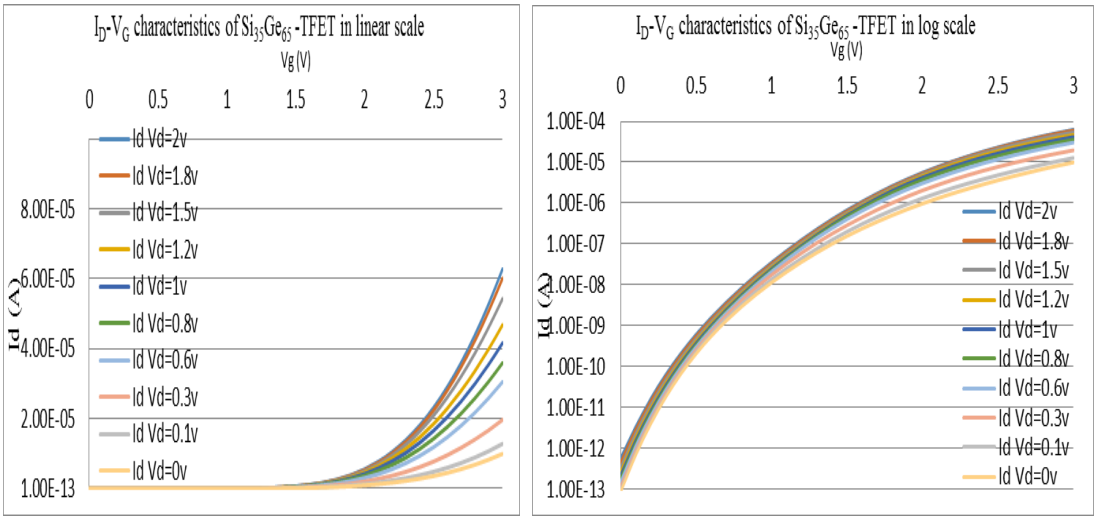


Figure 4.11: I_d-V_g characteristics of TFET using $Si_{35}Ge_{65}$ as body for various Vds in linear and log Scale.

Id-Vg characteristics for 0V<Vds<3V of the 32nm Npoly gate and SiGe body TFET are plotted on linear and logarithmic scale in Fig. 4.11. For SiGe TFET for V_{ds}=1.2V, I_{OFF}=1.48351e^{-12}µA/µm at Vgs=0Vand I_{ON}=6.99737e^{-05}µA/µm at Vgs=3V. Fig. 4.12 shows the C-V characteristics of MOSFET and TFET for different body material. The limiting factor for attaining high cut-off frequency is the low value of trans-conductance and a high gate-to drain capacitance (C_{gd}). The dynamic behavior of a device is the result of device capacitive effects caused by the charges stored in the device. Simulated graph shows that Si-TFET has lowest capacitance whereas SiGe-TFET has very high capacitance.

Comparison of C-V of MOSFET and TFET:

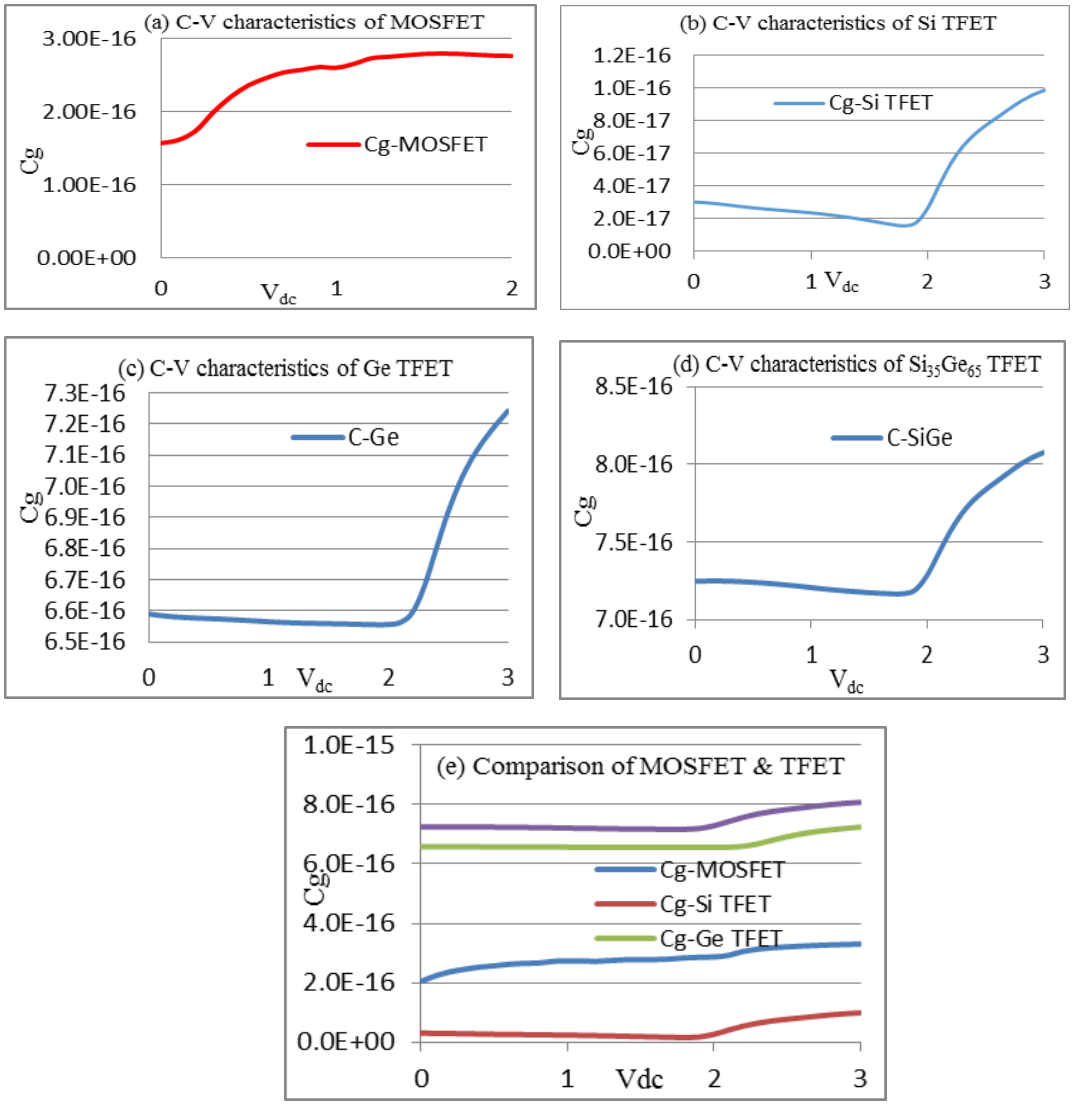
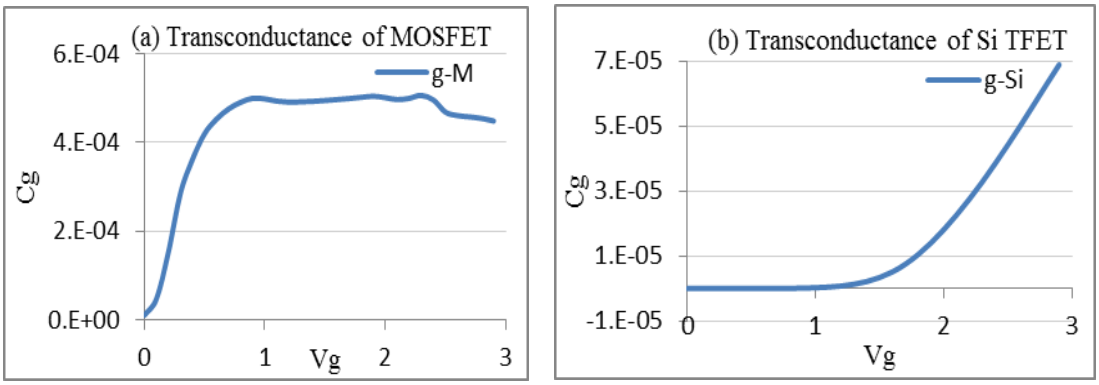


Figure 4.12: C-V characteristics of MOSFET and TFET: (a) MOSFET (b) TFET as Si body (c) TFET as Ge body (d) TFET as SiGe body (e) comparison of MOSFET & TFET.

Comparison of Transconductance of MOSFET and TFET:



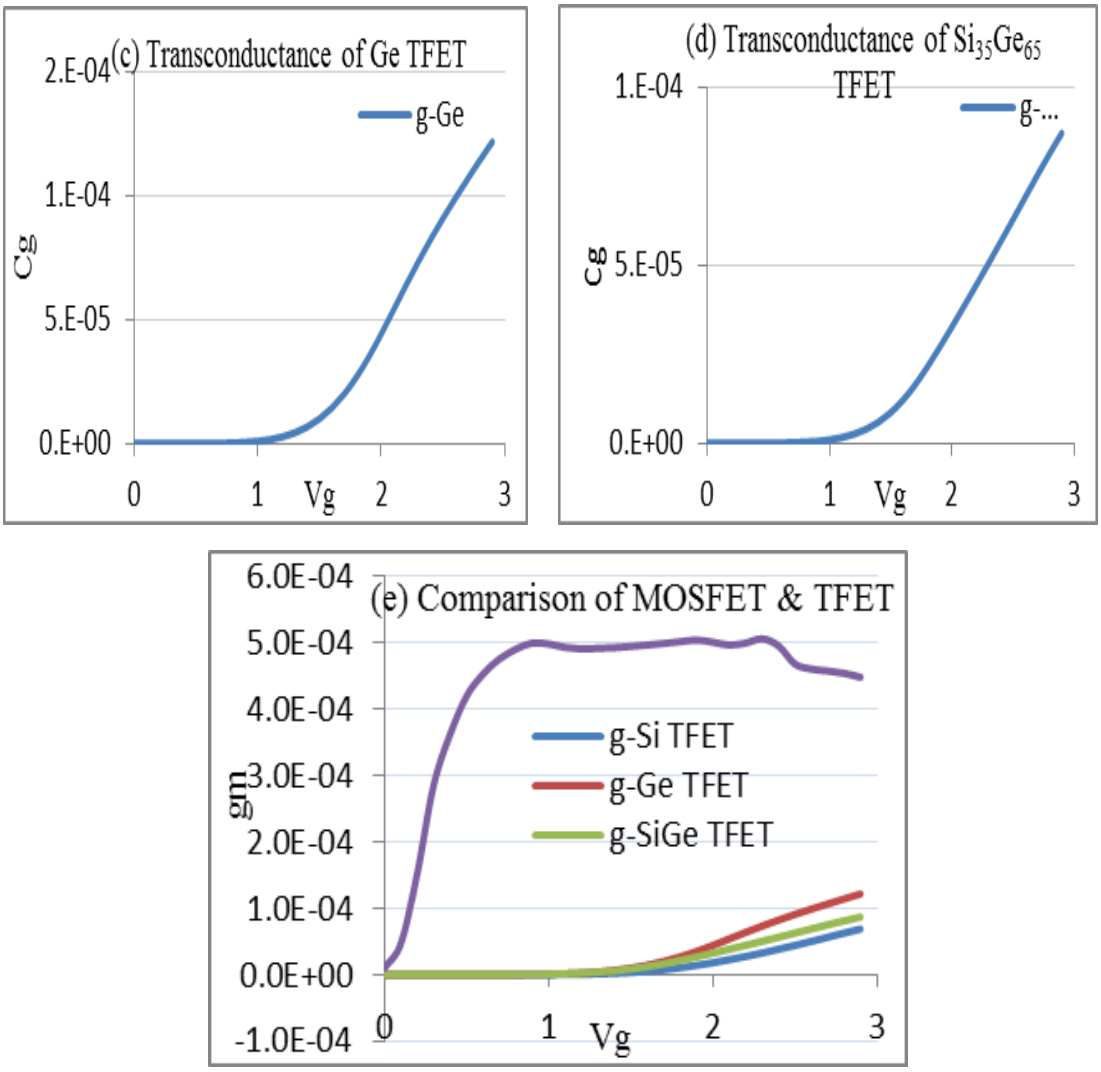


Figure 4.13: Transconductance: (a) MOSFET (b) TFET as Si body (c) TFET as Ge body (d) TFET as SiGe body (e) Comparison of MOSFET & TFET.

Above Fig. 4.13 shows the Transconductance of MOSFET and TFET. Transconductance of MOSFET is very high as compare to the TFET. Above graph shows the transconductance (*gm*) for TFET of different material. Since, Si, Ge and SiGe material is used for body Transconductance curve for these TFETs are plotted. Following section compared these graphs and it has been observed that *gm* of Si TFET is lower than Ge TFET and SiGe TFET has values that are between these two.

Comparison of PDP:

PDP shows how much power is consumed by the device at that particular delay. Combining these two parameters is important as these are the main performance parameters of the device.

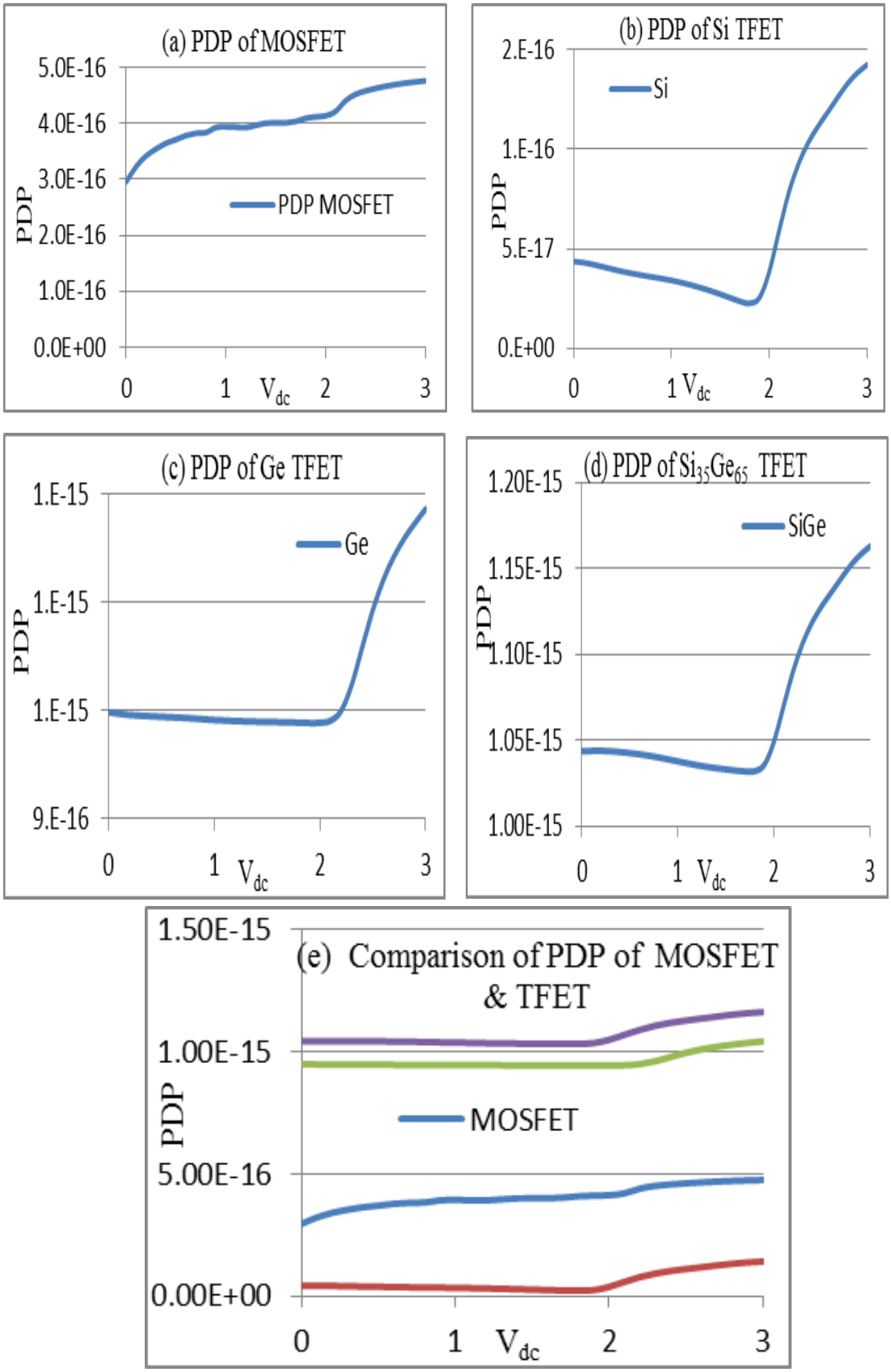


Figure 4.14: PDP: (a) MOSFET (b) TFET as Si body (c) TFET as Ge body (d) TFET as SiGe body (e) Comparison of MOSFET & TFET.

C) Analytical Calculations:

A. Calculation of PDP:

$$\textbf{PDP} = C_G \times V_{DD}^2 \quad \textbf{fJ/µm}$$

$PDP_{MOSFET} = 2.723e^{-16} \times (1.2)^2$ $= 3.922e^{-16}$fJ/µm	$PDP_{TFET\ Si} = 2.21e^{-17} \times (1.2)^2$ $= 3.183e^{-17}$fJ/µm
	$PDP_{TFET\ Ge} = 6.562e^{-16} \times (1.2)^2$ $= 9.449e^{-16}$fJ/µm
	$PDP_{TFET\ SiGe} = 7.191e^{-16} \times (1.2)^2$ $= 1.036e^{-15}$fJ/µm

B. Calculation of Time Delay (Ƭ):

$$Ƭ = \frac{Cg \times Vdd}{Ion} \quad fs$$

Time Delay of MOSFET $Ƭ = \frac{2.72332e-16 \times 1.2}{0.00128714}$ $Ƭ = 2.53894e-13\ fs$	Time Delay of TFET Si : $Ƭ = \frac{2.21046e-17 \times 1.2}{4.46133e-5}$ $Ƭ = 5.666235e-13\ fs$
	Time Delay of TFET Ge : $Ƭ = \frac{6.56196e-16 \times 1.2}{9.73722e-5}$ $Ƭ = 8.086858e-12\ fs$
	Time Delay of TFET $Si_{35}Ge_{65}$: $Ƭ = \frac{7.1912e-16 \times 1.2}{6.99737e-5}$ $Ƭ = 1.233240e-11\ fs$

C. Calculation of Subthreshold Swing (SS) V_{dd}=1.2V:

$$SS = \frac{Vdd}{\log\frac{ION}{IOFF}} \text{ mV/decade}$$

Subthreshold Swing (SS) for MOSFET	
V_{DD} = 0.6V	V_{DD} = 0.3V
$SS = \frac{0.6}{\log\left(\frac{0.0002}{5e-7}\right)}$ SS = 230mV/decade	$SS = \frac{0.3}{\log\left(\frac{1e-4}{1.956825e-6}\right)}$ SS = 175.57mV/decade
Subthreshold Swing (SS) for TFET	

V_{DD} = 1.2V	V_{DD} = 0.3V
Si TFET $SS = \frac{1.2}{\log\left(\frac{1e-7}{2.55e-13}\right)}$ SS = 214 mV/decade	Si TFET $SS = \frac{0.3}{\log\left(\frac{1e-7}{1.12016e-13}\right)}$ SS = 50.41mV/decade
Ge TFET $SS = \frac{1.1}{\log\left(\frac{1e-7}{4.5835e-11}\right)}$ SS = 329 mV/decade	Ge TFET $SS = \frac{0.3}{\log\left(\frac{1e-7}{6.59958e-12}\right)}$ SS = 71.76 mV/decade
$Si_{35}Ge_{65}$ TFET $SS = \frac{1.2}{\log\left(\frac{1e-7}{1.4845e-12}\right)}$ SS = 227 mV/decade	$Si_{35}Ge_{65}$ TFET $SS = \frac{0.3}{\log\left(\frac{1e-7}{6.01877e-13}\right)}$ SS = 57.46 mV/decade

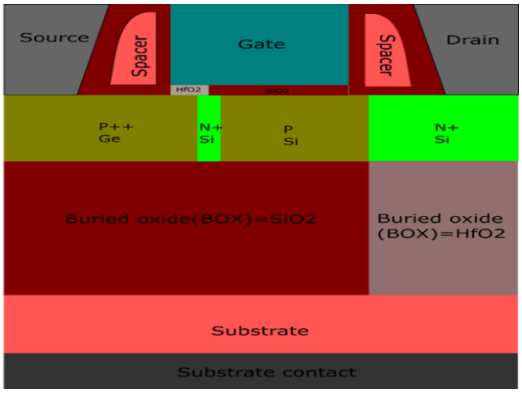
Table 4.3 gives a comparative summary of I_{ON} and I_{OFF} of MOSFET and TFET with different body material. MOSFET has I_{ON} in mA range whereas, TFET has I_{ON} in µA range. However, MOSFET has Large I_{OFF} than TFET. Among the different body material used in TFET $Si_{65}Ge_{35}$ has better I_{ON} current and its Delay time depends directly on the intrinsic capacitance and is inversely proportional to current. The delay time for MOSFET is less as compared to TFET, because the current level of MOSFET is high and the intrinsic capacitance is also minimum.

Table 4.3: Comparison of different parameter of MOSFET and TFET at V_{dd}=0.3V and V_{dd}=1.2V.

Sr. No.	**Device**	**I_{ON}** ↑ (A/µm)	**I_{OFF}** ↓ (A/µm)	**Subthreshold Swing (SS)** ↓ **(**mV/dec**)**		**Transconductance (gm) (S)** ↓	**PDP** ↑ (fJ/µm)	**Time Delay (**fs **)** ↑	V_{th} ↑ (V)
				V_{dd}=0.3 V	**V_{dd}=1.2V**				
1	MOSFET	**0.00128714 (A/µm)**	3.36348e-07 (A/µm)	175.57 mV/dec	230.00 mV/dec	**0.0004907 (S)**	3.922e-16 fJ/µm	**2.53894e^{-13} fs**	-
2	Si TFET	4.68133e^{-05} A/µm	**2.55896e^{-13} A/µm**	**50.41 mV/dec**	**214.00 mV/dec**	7.97e^{-07} S	**3.183e^{-17} fJ/µm**	5.666235e^{-13} fs	**0.96 V**
3	Ge TFET	9.73722e^{-05} A/µm	4.52214e^{-11} A/µm	71.76 mV/dec	329 mV/dec	2.752e^{-06} S	9.449e^{-16} fJ/µm	8.086858e^{-12} fs	1.25 V
4	$Si_{65}Ge_{35}$ TFET	6.99737e^{-05} A/µm	1.48351e^{-12} A/µm	**57.56 mV/dec**	227 mV/dec	2.574e^{-06} S	1.036e^{-15} fJ/µm	1.233240e^{-11} fs	1.03 V

C) Ge/Si Hetero-junction Hetero-gate PNPN TFET with Hetero-dielectric BOX to improve I_{ON}/I_{OFF}

This simulation work proposed a Ge/Si Heterojunction hetero-dielectric PNPN Tunnel FET which adds a hetero-dielectric BOX on the highly doped ground plane. Rather than utilizing p+ source as a part of an ordinary TFET, a tunneling junction is framed between the p+ area and a completely depleted thin n layer under the gate which decreases the tunneling width and makes nearby band bowing and in this manner a steep subthreshold slope is obtained. This n pocket enhances the tunneling by accomplishing steep subthreshold conduct and in the meantime gives high I_{ON} when contrasted with ordinary PNPN TFET utilizing Gate oxide made of HfO_2 (k=25) and SiO_2 (k=3.9)[91]. an optimal way to wipe out the ambipolar conduction in TFETs by utilizing a hetero-dielectric BOX over a vigorously doped (P+) substrate of a N-channel PNPN TFET. The proposed device design encourages the depletion of the drain area at the channel-drain interface expanding the tunneling obstruction width on the drain side bringing about the suppression of the ambipolar conduction [94]. Here Kane Band-to-Band Tunneling model is used in which value of two parameters of Kane's model are A. BTBT = $3.9e+22eV^{(-1/2)}cm^{-1}s^{-1}V^{-2}$ and B. BTBT = 2.25e+07 $Vcm^{-1}eV^{(-2/3)}$. A meshing is applied to the whole device to create the calculation points where the semiconductor equations are applied. Fig. 4.16 shows a mesh structure of the simulated PNPN TFET. It is visualized that meshing is dense near the gate oxide/source/channel tunnel junction, where actual tunneling in TFET occurs so that accurate values of current and voltages can be predicted.



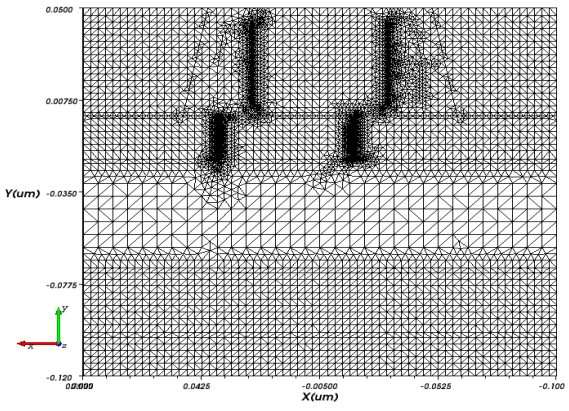


Figure 4.15: Structure of PNPN TFET. Figure 4.16: Mesh structure of the PNPN TFET.

Before, finalizing proposed device parameters, conventional device is simulated and various parameters are varied to analyze which device gives the best performance. Simulations are done at Vds=1.2V and Vgs is varied from 0 to 2.5V. In the proposed device two dielectrics materials are used for gate oxide namely: High-k HfO_2 and Low-k SiO_2 hetero-dielectric. The Plot of Id-Vg characteristics for various HfO_2 lengths are shown in Fig. 4.17.

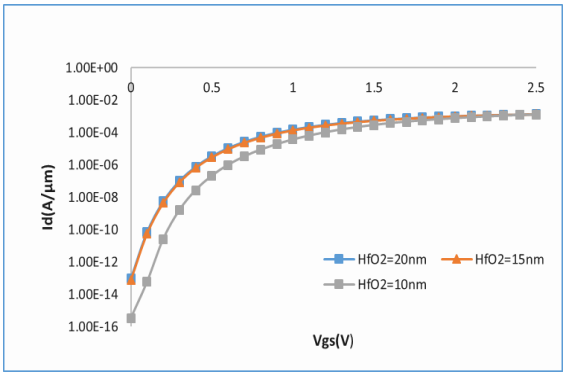


Figure 4.17: Id-Vg characteristics of HfO_2 length variations.

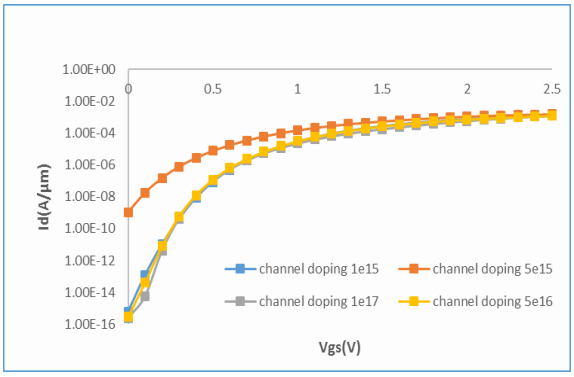


Figure 4.18: Channel doping variations.

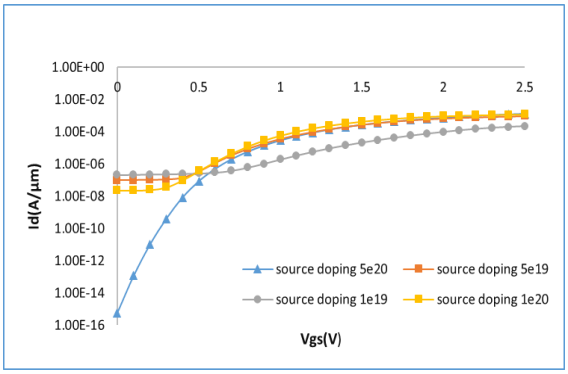


Figure 4.19: Source doping variations.

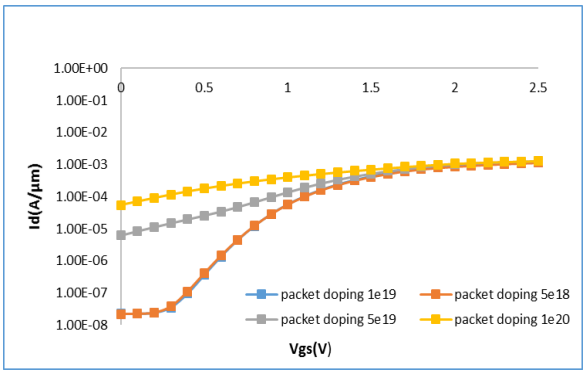


Figure 4.20: N packet doping variations.

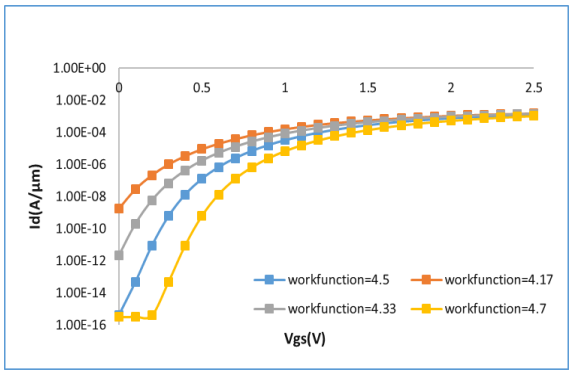


Figure 4.21: Work function variations.

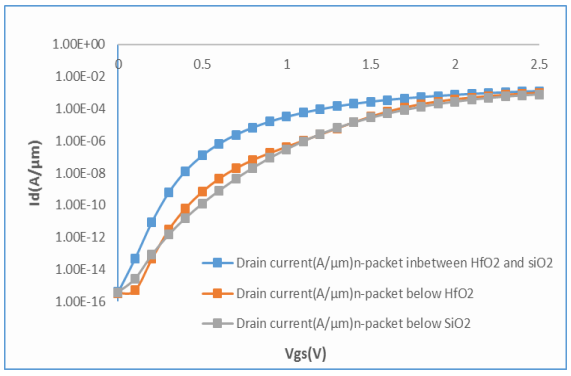


Figure 4.22: N packet position variations.

Higher I_{ON} is obtained at 10nm technology node. To ponder the impact of channel doping on device performance, the channel doping is varied, keeping source and drain doping to 5e+20 atoms/cm^{-3} and 5e+18 atoms/cm^{-3} respectively. The proposed device is N- type Tunnel FET, in which channel region is n type doped. Nd concentration is varied from 1e+15, 5e+15, 1e+16, 5e+16 and 1e+17 atoms/cm^{-3}. Drain current values for channel doping with 5e+15atoms/cm^{-3} are better among them. There is not much difference in the Id-Vg characteristics for these values as indicated in Fig. 4.18. At 5e+20atoms/ cm^{-3} have better drain current for source doping as shown in Fig. 4.19. Also n packet doping varies with 1e+19, 5e+18, 5e+19 and 1e+20 atoms/cm^{-3}. Among them 1e+19 shows better I_{ON} as shown in Fig. 4.20. The alternative variations in work function for 4.17, 4.33, 4.7 and 4.5eV where analyzed; 4.5eV shows steeper performance as indicated in Fig. 4.21. When the position of the N packet which is extra layer in PNPN is changed, it changes its Id-Vg characteristics and it shows superior performance under half of HfO_2 and half of SiO_2 as drawn in Fig. 4.22. The simulated device parameters are listed in Table 4.4 which indicates region materials, contact materials, region thickness/length and doping concentrations of the regions. Gate material is of NpolySi.

Table 4.4 Design parameters of the device.

Region	**Contact material**	**Material**	**Thickness/ Length**	**Doping (Atoms/cm^3)**
Source	Al	Ge	50nm	N_A (P++ type) 5×10^{20}
Drain	Al	Si	50nm	N_D (N+ type) 5×10^{18}
Channel	-	Si	50nm	N_D (N type) 5×10^{15}
N pocket	-	Si(4nm)	20nm	N_D (P type) $1x10^{19}$
Substrate	Al	Si	30nm	N_A (P type) $1x10^{17}$
Buried Oxide	-	SiO_2(136nm) +HfO_2(54nm)	50nm	-
Gate Oxide	-	HfO_2(10nm) + SiO_2(40nm)	4nm	-
Spacer	-	Nitride	20nm	-

By utilizing materials with smaller band gaps, the on-state current of a TFET could be greatly improved.

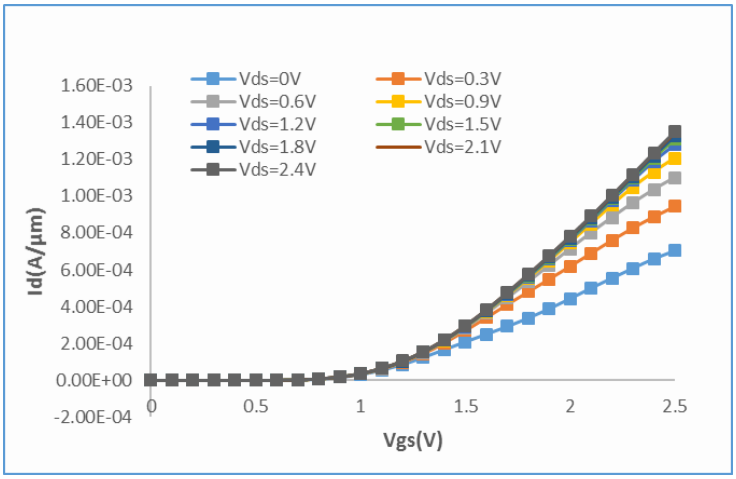


Figure 4.23: Id-Vg characteristics.

Fig. 4.23 shows that by varying Vds from 0V to 2.4V; the plot of Id-Vgs are analyzed. These values predict that, for different values of Vds, Id value varies in a small fraction. It means that the proposed device doesn't show any DIBN effect [93].

The Ge/Si Heterojunction hetero-gate dielectric with hetero-dielectric BOX PNPN Tunnel FET with low bandgap material at source region increases the tunneling probability and hence improves I_{ON}. With the different variations of channel, source, drain and N pocket doping, optimized value from Id-Vg characteristics. Also, the work function is varied for exploring the possibilities of improvement of I_{ON} and reduction of I_{OFF}. Hetero gate dielectric improves the I_{ON} and suppresses the ambipolar current. Also DIBN effect gets reduced because drain current is not varied with changes in Vds(V) values with respect to Vgs(V) values. Hetero-dielectric Buried Oxide (BOX) layer reduces the parasitic capacitance and reduces the leakage currents and also suppress the ambipolar behavior. $I_{ON}/I_{OFF}=3.47\times10^{12}$, SS=44.66mV/dec obtained is better than [93].

From this study, it is concluded that PNPN TFET with low band-gap materials and with the combinations of hetero-dielectric is the promising key alternative for high speed low power FPGA applications. In future, with the help of low band gap materials like SiGe/Si with varied concentration PNPN TFET can be designed.

D) Performance analysis of TFET using Si0.35Ge0.65/Si Hetero-junction Hetero-dielectric with Buried Oxide layer

A higher ON-state current for a TFET can be achieved by utilizing smaller band gap material. However, this can additionally increase the OFF-state leakage current [95-97] because TFET shows ambipolar behaviour, meaning for negative gate bias, conduction happens at the drain/channel junction. The ambipolar behaviour of TFET can be suppressed if completely different doping is used for drain and source region creating uneven architectures, together with completely different gate materials with high k dielectric at the source side. Besides utilizing materials with smaller bandgaps, hetero-junction devices may even be adopted. Using a small band gap type material as the source material, the device on-state current could be improved [98].

Channel and drain regions are made with materials with a larger band gap so that drain side tunnelling leakage could be suppressed. $Si_{1-x}Ge_x$ is an attractive material for increasing the tunnelling probability of TFETs due to its lower energy bandgap [99-103]. According to the 2005 ITRS interest for the 50nm hub, I_{ON} should be 0.612mA/μm and I_{OFF} should be 10pA/μm [104-105]. To achieve this ITRS [105, 116] requirement, higher I_{ON} of 1.27mA/μm and I_{OFF} of 10.58fA/μm is effectively accomplished. The device is contrasted and homo-junction TFET structure with Si, Ge and SiGe as thin film body material also with different hetero-junction TFET by changing source material to Ge. The I_{ON}, I_{OFF}, SS, switching delay, PD and PDP of these devices are compared. With the proposed device a higher I_{ON} was acquired when contrasted and other TFET structures.

A proposed device structure of SiGe/Si hetero-junction TFET is shown in Fig. 4.24 which has SiGe Source with heavy P-type uniform doping, channel/drain of same Si material with channel slightly N-type uniform doped and drain heavy N-type uniform doped. Gate oxide made of both HfO_2 (k=25) and SiO_2 (k=3.9) hetero-dielectric. It is isolated from the substrate by 150nm SiO_2 Buried Oxide (BOX) layer which suppresses the leakage currents. Gold (Au) material is used for Gate, Source and drains contact. The thickness of SiGe/Si thin film ($_{body}$) is 20nm, Gate oxide thickness (t_{ox}) is 4nm, channel length (L) is 50nm and Gate work-function (φ_m)=4.7eV. The detailed proposed device parameters are listed in Table 4.5. Kane BTBT model is used in which value of two

parameters of Kane's model given in inbuilt help documentations of software are, A. BTBT=3.9e+22 $eV^{(-1/2)}cm^{-1}s^{-1}V^{-2}$ and B. BTBT = 2.25e+07 $Vcm^{-1}eV^{(-2/3)}$. Also a mobility model like Lombardi mobility model is used. A meshing is applied to the whole device to create calculation points where the semiconductor equations are applied. Fig. 4.25 shows a mesh structure of the simulated TFET.

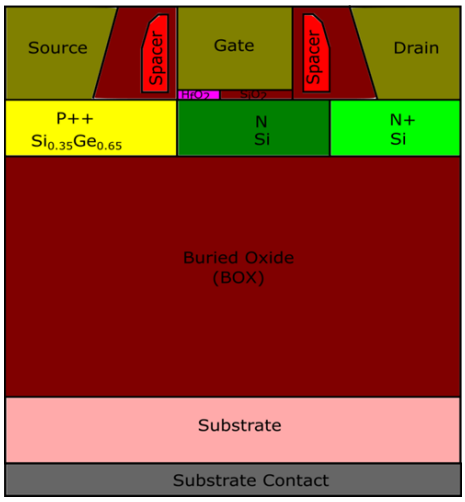


Figure 4.24: Design Structure of Simulated TFET.

Table 4.5 Design parameters of the simulated device.

Region	**Material**	**Contact material**	**Thickness / Length**	**Doping (Atoms/cm^3)**
Source	$Si_{0.35}Ge_{0.65}$	Au	70nm	N_A (P++ type) 5×10^{20}
Channel	Si	-	50nm	N_D (N type) 5×10^{15}
Drain	Si	Au	54nm	N_D (N+ type) 5×10^{18}
Substrate	Si	Al	30nm	N_A (P type) $1x10^{17}$
Gate Oxide	HfO_2(20nm)+ SiO_2(30nm)	-	4nm	-
Buried Oxide	SiO_2	-	150nm	-
Spacer	Nitride	-	30nm	-

When meshing is applied, the TCAD simulation software automatically predicts the junction points and finer mesh is applied to the region. Before finalizing proposed device parameters, conventional device is simulated and varied various parameters to

obtain better device performance. Simulations are done at Vds=1.2V, Vgs is varied from 0 to 2.5V and Gate work-function=4.7ev is used.

In proposed device, compound $Si_{1-x}Ge_x$ material is used as a source which is a low energy gap material where x represents the percentage composition of Ge. Energy gap decreases as with increase in the x values [14]. Fig. 4.26 shows a plot of Id-Vg characteristics for various germanium contents (x) values and reflects that the characteristics are not steeper and leakage current is more for lesser values of x. However, increases in the percentage composition of germanium (x value increases), results in steeper Id-Vg characteristics. It is because band gap (tunnelling distance) decreases with increasing x values. So, in proposed device, the value of x=0.65 is chosen.

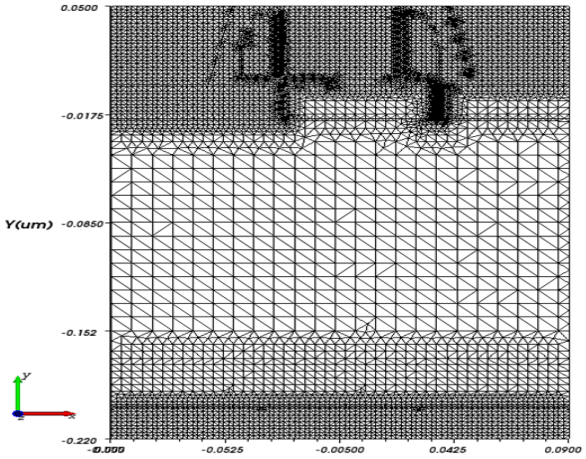


Figure 4.25: Mesh structure of the simulated TFET.

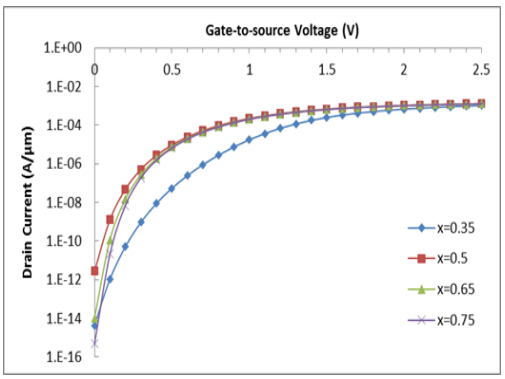


Figure 4.26: Id-Vg for various Ge content (x) values.

Channel, Source and Drain doping variation

To study the impact of channel doping on device performance, the channel doping is varied, keeping source and drain doping to 5e+20 atoms/cm^{-3} and 5e+18 atoms/cm^{-3}

respectively. With intrinsic channel, the Id-Vg characteristics are not steeper, however, results in very low OFF current as shown in Fig. 4.26. A proposed device is N- type TFET, in which channel region is n-type doped. N_d concentration is varied from 5e+15, 5e+16 and 5e+17 atoms/cm^{-3}. As seen from the plot, characteristics are steeper and drain current has been increased for all varied values of N_d. Drain current values for channel doping with 5e+15atoms/cm^{-3} are better among them. There is not much difference in the Id-Vg characteristics for these values. Additionally, the effect of Source and Drain doping on the device execution is also considered. Channel doping constant is used as 5e+15 atoms/cm^{-3} and varied the source and drain doping concentration. The Id-Vg characteristics plot for various source and drain doping combination is shown in Fig. 4.27. To make asymmetric architecture source and drain doping must be different which help to suppress the ambipolar behavior of TFET. As seen from the plot, it is observed that source is heavily doped than the drain. for the source doping (N_A) of 5e+20 atoms/cm^{-3} and drain doping (N_D) of 5e+18 atoms/cm^{-3}, Id-Vg characteristics are steeper and have higher drain current.

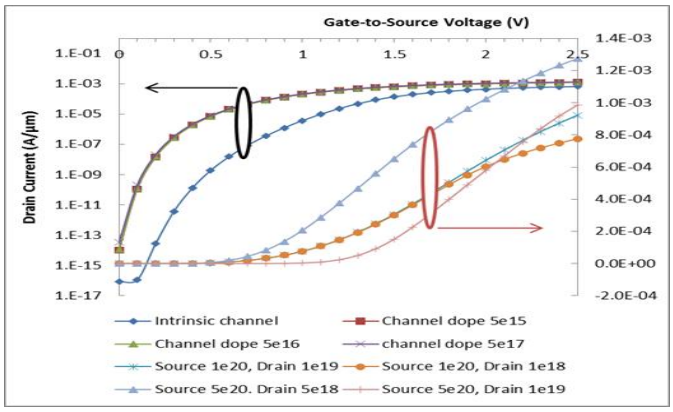


Figure 4.27: Id-Vg for the various channel, source and drain doping variation.

Gate Work Function variation

Work function 'φs' describe the energy cost of removing an electron from the material. Gate work-function is an important parameter which affects the V_{th} of device [107]. From Simulation results it can be observed that by setting proper gate wok-function, higher drain current and low V_{th} can be obtained. Id-Vg characteristics is plotted for various values of φs as shown in Fig. 4.28 for φs = 4.17eV, Id-Vg curves are as shown in Fig. 4.27. It has very low I_{OFF}, but V_{th} is shifted to larger values as

characteristics are not steep. As the value of work-function increases, characteristics become steeper, and V_{th} gets reduced for φs=4.7eV, as shown in the plot.

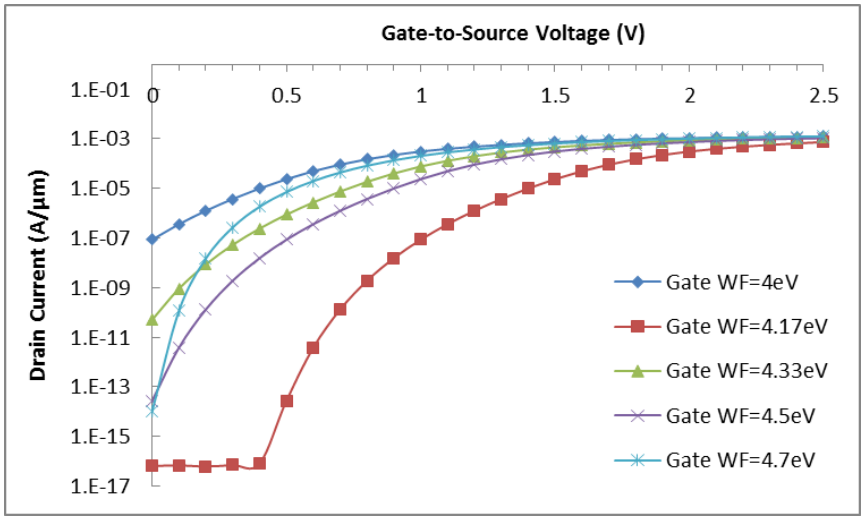


Figure 4.28: Id-Vg for various Gate work-functions.

Homo-junction and hetero-junction comparison

In hetero-junction TFET, Source region is of a different material than the channel/drain region. As tunnelling happens at source/channel junction in N-type TFET, the source must be low vitality bandgap material to diminish the tunnelling separation that will expand the tunnelling current. Table 4.6 gives the physical properties of Si, Ge, and $Si_{1-x}Ge_x$. Ge and $Si_{0.35}Ge_{0.65}$ have a low energy gap, high electron/hole mobility than the Si. Therefore, in this work $Si_{0.35}Ge_{0.65}$ and Ge are used as source material.

Table 4.6. Physical properties of Si, Ge and SiGe.

Properties	**Si**	**Ge**	**$Si_{0.35}Ge_{0.65}$**
Indirect Energy Gap (eV) at 300K	1.12 (a*)	0.66 (a*)	0.85 (a*)
Dielectric constant at 300K	11.7 (a*)	16.2 (a*)	14.6 (a*)
Lattice constant (nm)	0.5431 (a*)	0.5657 (a*)	0.5572 (a*)
Electron affinity (eV)	4.05 (b*)	4.00 (b*)	4.02 (b*)
Melting Point (^oC)	1412 (a*)	937 (a*)	1043 (a*)
Mobility (cm^2/Vs)	Electron-1500 Hole-450 (b*)	Electron-3900 Hole-1900 (b*)	Electron-3025 Hole-1392.5(b*)

Footnote: a*- [108], b*- [109]

Id-Vg characteristics of hetero-junction is compared with homo-junction TFET as shown in Fig. 4.29. As seen from the plot, SiGe/Si hetero-junction TFET, and Ge/Si hetero-junction TFET have many similar Id-Vg characteristics. It is observed that SiGe/Si hetero-junction TFET has little better characteristics than Ge/Si hetero-junction TFET.

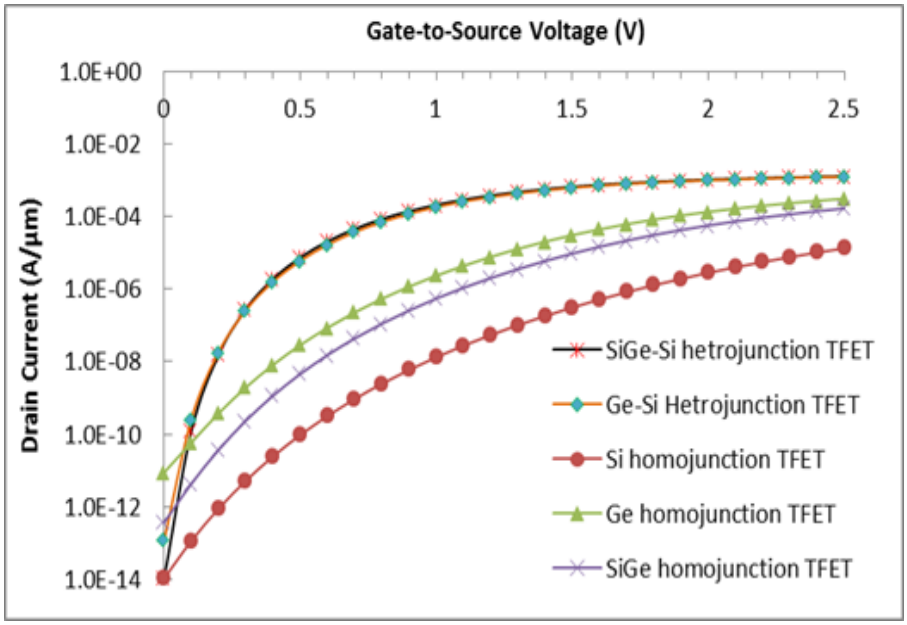


Figure 4.29: Comparison of Id-Vg characteristics of hetero-junction and homo-junction TFETs.

It can be seen from the plot that Si homo-junction TFET have very low I_{ON} in the µA range and large SS. It is because of the large energy band-gap of silicon that limits the tunnelling current. So, different low energy gap material is used in the body like Ge and SiGe compound material. Improvement in the Id-Vg characteristics is observed, but as TFET shows ambipolar behaviour, its I_{OFF} also increases. This is the demerit of homo-junction TFET. So SiGe/Si hetero-junction TFET is designed and simulated which shows very steep Id-Vg characteristics, higher I_{ON}, low I_{OFF} and low SS as seen from the plot.

Electrical Characteristics of Proposed Device

The N-type Tunnel FET is switched ON once $Vgs>V_{th}$. Our proposed devices have the structure of p-i-n diode that is normally turn around one-sided in OFF-state so leads to an ultra-low leakage current. As the gate voltage increases positively, it leads to associate in nursing accumulated n-region below the gate oxide and current starts to flow across the device [19]. This section simulated device at a drain-to-source voltage (Vds) of

1.2V and gate-to-source voltage (Vgs) is varied from 0 to 2.5V. Energy band diagram of proposed device is as shown in Fig. 4.30.

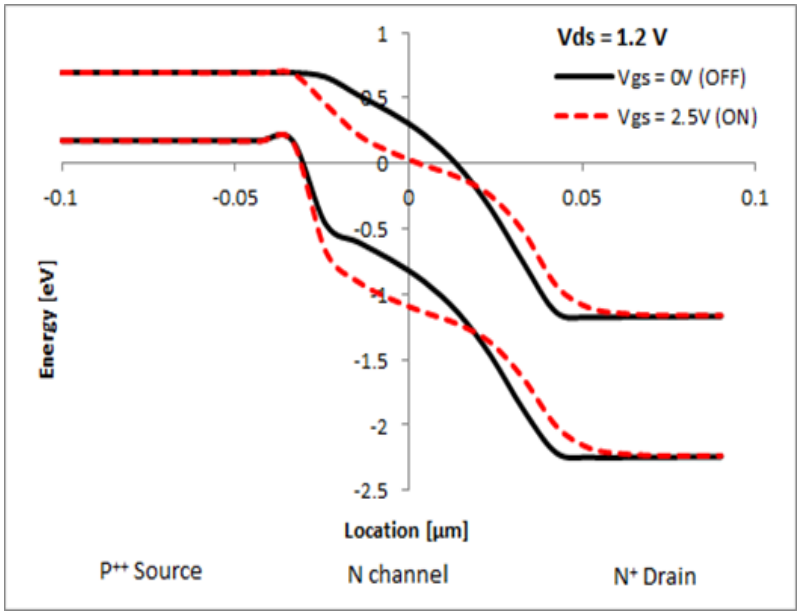


Figure 4.30: Energy band diagram of proposed TFET in OFF and ON condition.

When TFET is in OFF-state i.e., Vgs=0V, TFET is reverse biased which ends up in larger tunnelling barrier width. A high-K HfO_2 dielectric oxide is used near source/channel junction due to which valance band of the channel near source end has been increased. This reduces the tunnelling probability, and results in reduced I_{OFF}. Once TFET is in ON state i.e. Vgs=2.5V, electrons begin tunnelling from valance band of P++ source to the conduction band of the N-channel then towards the conduction band of the N+ drain region [110].

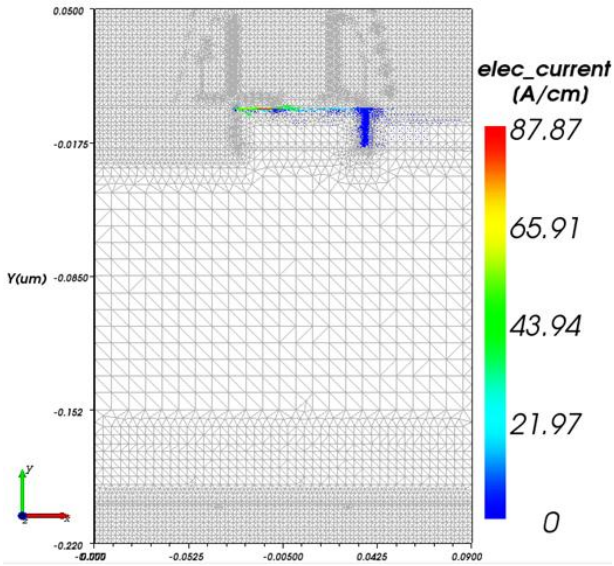


Figure 4.31: Flow of electron current in TFET at Vgs = 2.5V and Vds = 1.2V.

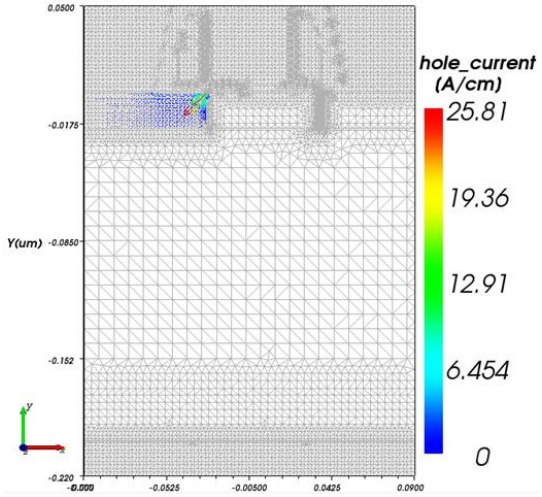


Figure 4.32: Flow of hole current in TFET at Vgs = 2.5V and Vds = 1.2V.

It has been observed that the flow of electron within the device at Vgs = 2.5V as shown in Fig. 4.32. In n-type TFET tunnelling occurs at the surface close to the Gate Oxide/channel/source region where maximum current flows. From simulated schematic, it can be watched that electrons tunnel from the surface of source region into the channel beneath the gate oxide area and after that stream into the drain region. The hole current is opposite to the electron current [89]. The hole current flows from drain region into the channel and then flow into the source region as shown above.

When V_G is increased positively, potential near-source/channel junction increases due to which tunneling of current occurs. It can also be seen from the plot that potential near channel drain region is decreased which blocks the leakage current and suppress the ambipolar behaviour of TFET.

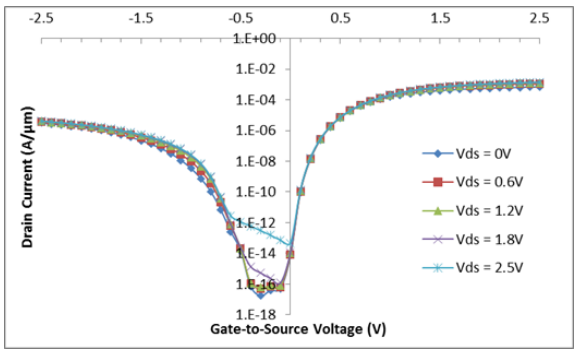


Figure 4.33: Id-Vg characteristics of proposed device.

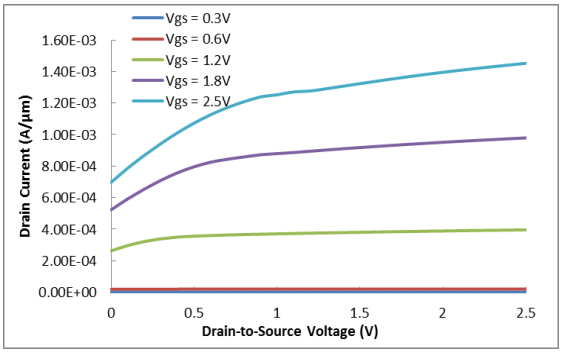


Figure 4.34: Id-Vd characteristics of the proposed device.

In N-TFET, for positive gate bias, the device operates in N-mode of TFET, where tunnelling occurs at source and channel junction. However, when negative gate bias is applied to the same device; it works in P-mode [110]. In this mode, tunnelling occurs at drain/channel junction. Fig. 4.33 shows Id-Vg a characteristic of proposed device in which gate is biased from negative to a positive voltage for various drain-to-source (Vds) voltages. The drain current is reduced in P-mode of TFET as seen in the plot; this is due to suppressed ambipolar behaviour of the device using high-K dielectric and hetero-junction. Varying Vds voltage from 0V to 2.5V, Id-Vd characteristics is plotted for various Vgs as shown in Fig. 4.34. The output characteristic of proposed TFET indicates high I_{ON}.

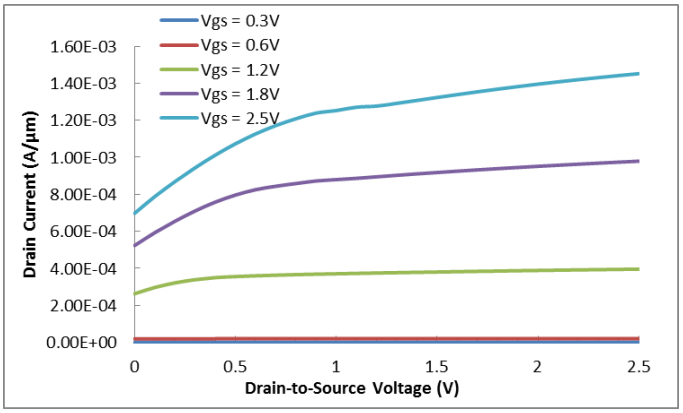


Figure 4.35: Id-Vd characteristics of the proposed device.

Comparison of simulated devices

Table 4.7 Comparison of performance parameters of simulated devices.

Parameter	$Si_{0.65}Ge_{0.35}$ Homo-junction TFET	Ge/Si Hetero-junction TFET	$Si_{0.35}Ge_{0.65}$/Si Hetero-junction TFET
I_{ON} (mA/μm)	0.165	1.244	1.276
I_{OFF} (fA/μm)	366	117.70	10.58
I_{ON}/I_{OFF} ($\times 10^{11}$)	0.0045	0.1	1.2
SS (mV/dec)	145	47.4	40.4
Switching delay (psec)	575	3.50	3.16
Power dissipation (pWatt)	13.8	14.4	14.3
PDP($\times 10^{-23}$J/μm)	798	5.04	4.51

Various performance parameter of the proposed device is compared with other TFET structures. From the electrical characteristics, extracted I_{ON}, I_{OFF}, SS, switching delay, power dissipation and PDP from simulated information are shown in Table 4.7.

Subthreshold Slope/Swing (SS)

The SS is an important property of TFET wherein smaller is the value of S; better is the dynamic performance. Subthreshold Swing/Slope can be described as the Vgs required for change of a magnitude of drain current to turn the device from OFF state to ON state. It can be determined as the inverse of the slope of the log Ids Vs Vgs curve, in the sub-threshold exponential region [111].

$$SS = \frac{\partial V_{gs}}{\partial(\log I_d)} \quad \text{.....(4.1)}$$

The switching speed of a device is determined by SS [110].

Switching Delay

Switching delay is given by [109].

$$t_{delay} = \frac{C_{g,avg} V_{dd}}{I_{ON}} \quad \text{.....(4.2)}$$

Where, $C_{g,Avg}$ is the average capacitance across the gate bias (from 0 to V_{DD}=Vds).

Dynamic Power Dissipation

It is dissipated power in the device when it is in ON state. In simulation, 10KHz frequency is used to calculate the gate capacitance.

$$P_{dynamic} = C_{g,avg} V_{dd}^2 f \quad \text{.....(4.3)}$$

Power Delay Product

PDP represents Power-Performance trade-off at given operation frequency and is given by [106].

$$PDP = C_{g,avg} {V_{dd}}^2 f \times t_{delay} \quad \text{.....(4.4)}$$

All parameters are extracted for Vds=1.2V. The I_{ON} is extracted for the value of the drain current at a gate voltage of 2.5V. The I_{OFF} is extracted for the value of drain current at Vgs=0V.

From all simulation results and its interpretation, the upsides of a SiGe/Si hetero-structure are distinguish, and are as follows,

- Steeper SS.
- Lower bandgap in SiGe results in larger tunnelling current contrasted with the Si.
- Low power dissipation and High switching speed.
- The bigger bandgap at the drain-channel junction in Si results in little tunnelling current which diminish the ambipolar conduct.

These focal points make the hetero-structure TFET a promising contender for low power application and logical switching which needs steep SS and higher tunneling current.

4.3 Summary

Low bandgap material at source increases the tunnelling probability and thus improves the I_{ON} current. Subsequently, in this work, a hetero-junction hetero-dielectric TFET with SiGe as Source material is proposed and examined utilizing Cogenda TCAD device simulation programming. Hetero and homo-junction TFETs are compared and it has been observed that proposed SiGe/Si hetero-junction TFET has I_{ON} of 1.27mA/µm, I_{OFF} in fA/µm range, SS of 40mv/dec, switching delay of 3.16 pSec, power consumption

of 14.3pW and PDP of 4.51×10^{-23}Joules. The gate work-function is varied and found that it is an important parameter that can improve the I_{ON} and suppress the I_{OFF} of TFET. HfO_2 near the source side as gate oxide material reduces the energy band gap at a source-channel region which gives steep Id-Vg characteristics and enhances the sub-threshold slope. BOX layer decreases the parasitic capacitance and diminishes the leakage currents furthermore suppress the ambipolar conduct. Thus $Si_{0.35}Ge_{0.65}$/Si hetero-junction TFET with high-K dielectric oxide near source demonstrates a unique electrical trademark and fit for surpassing the TFET devices explored so far and could be a conceivable contrasting option to be utilized for the low power and fast FPGA applications.

Next Chapter deals about the performance evaluation of conventional Cu and emerging interconnects.

Chapter 5

PERFORMANCE EVALUATION OF EMERGING INTERCONNECTS

Interconnects principally decides the execution of frameworks at scaled innovation hub because of the expansion in chip measure and moderate scaling of interconnect measurements contrasted with the dynamic devices. While the execution of subthreshold circuits is extraordinarily enhanced as far as speed and power [3, 5, 20, 113-115], almost no advance has been made to enhance the execution of interconnects under subthreshold conditions [19, 116]. Henceforth, interconnect for subthreshold circuits should be additionally investigated and upgraded. Accordingly, this section basically concentrates on the outline of fast interconnects for vitality productive circuits. The initial segment presents diverse sorts of CNT interconnects alongside their benefits and constraints. The second part at that point looks at the execution of Cu and SWCNT interconnects for various biasing voltages in the subthreshold administration. At long last, the execution correlation amongst Cu and MCB interconnects is done under subthreshold conditions.

5.1 Introduction

The limit of interconnect is to scatter clock and different flags and to give power and ground lines to the distinctive circuits/system takes a shot at a chip. The width of the conducting lines that interface diverse transistors in a circuit is getting to be noticeably littler and littler as the innovation propels; in 2008, it dipped under 100nm, and now is of the request of a couple of many nm. As the gadget measurements are downsized so is that of interconnects.

Nonetheless, the presentation of Cu was not adequate for the important diminishment of RC delays. The National Technology Roadmap for Semiconductors (NTRS) and the ITRS expressed that materials with bring down dielectric constants would be required for wire protection as the element sizes of IC devices wound up plainly littler. The NTRS projected that within 10 years the industry should be able to achieve a standard dielectric constant of less than 1.5 in their production interconnect

material. However, the real situation has been much more challenging and complicated. As indicated by late versions of the ITRS, low-k materials with dielectric constants still as high as k = 2.5 were relied upon to be coordinated in 2012. One of the real purposes behind the Interconnect to confine the execution of a circuit is the RC impact.

Table 5.1 Comparison of different interconnects solution.

Solution	**OI Interconnects**	**CNT Interconnects**	**GNR Interconnects**
Method	• Using light as the main driving force instead of electrons, with the help of optical fibers, modulators and detectors.	• Using CNTs as wires instead of metallic material, ballistic conductors.	• Graphene is single carbon atom thick sheet. Layer of sheet as ballistic conductors
Advantages	• High propagation speeds. • High bandwidth, Provides chip to chip as well intra chip communication. • Low power and latency. • Noise immunity.	• Very high current carrying capability. • High thermal conductivity. • Electromigration resistant.	• Very high current density. • Support ballistic transport. • Planner growth. • Electromigration resistant.
Disadvantages	• Specialized components such as transmitter / receiver circuits are needed. • Benefits only for long lines. • Integration issues.	• Chirality control • Control of placement • Substrate interaction	• Control of edges • Single layer GNR has high resistivity. • Substrate interaction

5.2 Interconnect Simulations Executed

This section presents the simulation test bench used for performance analysis and comparison of Cu, CNT and GNR interconnects. Fig. 5.1 shows HSPICE test setup, the Driver Interconnect Load (DIL) system used for performance evaluation of CMOS, CNFET, FinFET and TFET driver with Cu, SWCNT, MWCNT, MCB and MLGNR interconnect for 32nm technology node at a frequency of 0.1GHz with a load capacitance of 1fF.

Figure 5.1: DIL system.

5.2.1 Parameters evaluated

32nm metal gate/high-k CMOS transistor PTM model, 32nm FinFET model, universal TFET model and circuit-compatible CNFET model from Stanford University [117, 118] are used for interconnect analysis. Equivalent RLC circuit models for Cu, SWCNT, MWCNT and MLGNR as shown in (Fig. 5.2–5.6) are used as interconnects. Carbon Nanotube Interconnect Analyser (CNIA) [119] is a tool used for extracting the RLC parameters of CNT. Graphene Interconnect tool is used for extracting RLC parameter of MLGNR. Furthermore, the RLC parameters of Cu were removed from PTM apparatuses with interconnect geometry parameter open in [119] for 32nm hub. A Simplified proportional RLC display for Cu interconnect is appeared in Fig. 5.2 having R-Resistance per unit length (p.u.l), L - Total Inductance of wire, C - Total capacitance of wire.

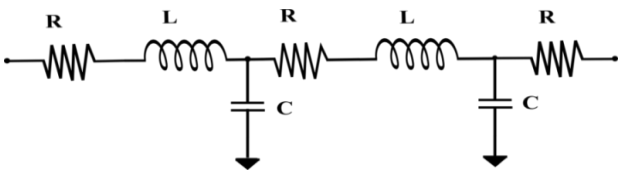


Figure 5.2: Cu interconnect RLC model for local, intermediate and global interconnects.

A Simplified corresponding RLC model of CNT interconnect for length not as much as the Mean Free Path of electron is showed up in Fig. 5.3. CNT has basic (quantum) protection (Rf) of 6.54KΩ and that can't be dismissed which is similarly isolated on the two sides of interconnect terminals. L – Total inductance of wire (kinetic + magnetic), C – Total capacitance of wire (quantum + electrostatic).

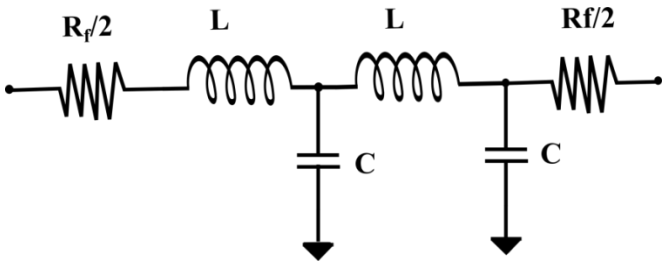


Figure 5.3: CNT interconnect RLC model for local interconnects (L < λ).

A Simplified equal RLC model of CNT interconnect for length bigger than the Mean Free Path of electron is appeared in Fig. 5.4. Here RCNT is the protection per unit length (p.u.l) of wire.

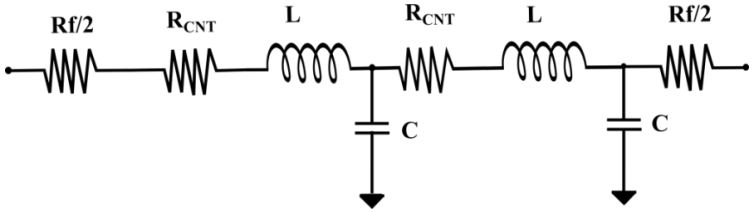


Figure 5.4: CNT interconnect RLC model for intermediate and global interconnects (L>λ).

A Simplified equivalent RLC model of GNR interconnect for local, intermediate and global is shown in Fig. 5.5. R_Q is the quantum resistance of GNR which is 12.9 KΩ/N_{ch}, where N_{ch} is number of conducting channels. R_{GNR} is resistance per unit length.

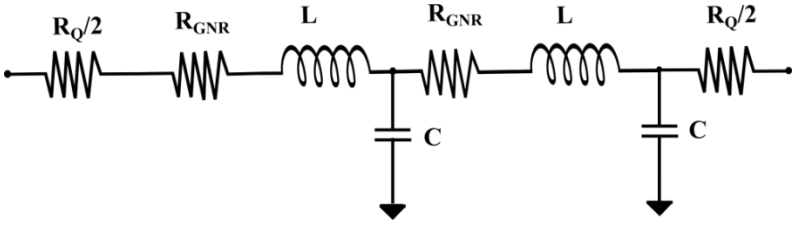


Figure 5.5: GNR interconnect RLC model for local, intermediate and global interconnects.

Netlist was written in HSPICE software to simulate the test bench. Fig. 5.6 shows an example of test bench used for evaluating the performance parameter of Cu interconnect incorporated with CMOS inverter driver and terminated with other CMOS inverter and load capacitor. Similarly, test bench for CNT and GNR interconnect with different device invertor driver is used. The W/L ratio used for CMOS, FinFET, CNFET and TFET device are as follows:

- For local level interconnect (N: P) (1:1.6) for CMOS, FinFET and TFET and (N: P) (30:30) no of CNT for CNFET.
- For intermediate level interconnect (N: P) (30:48) for CMOS. FinFET and TFET and (N: P) (120:120) no of CNT for CNFET.
- For global level interconnect (N: P) (50:80) for CMOS, FinFET and TFET and (N: P) (240:240) no. of CNT for CNFET.

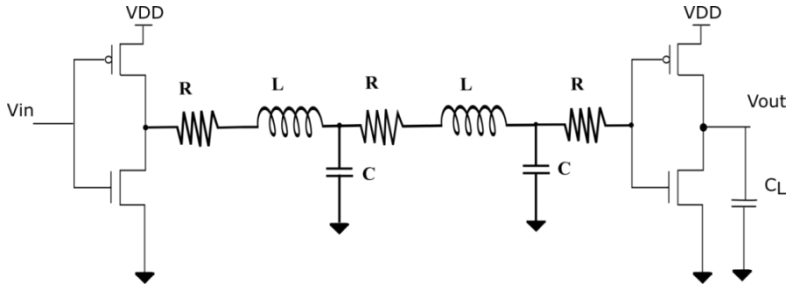


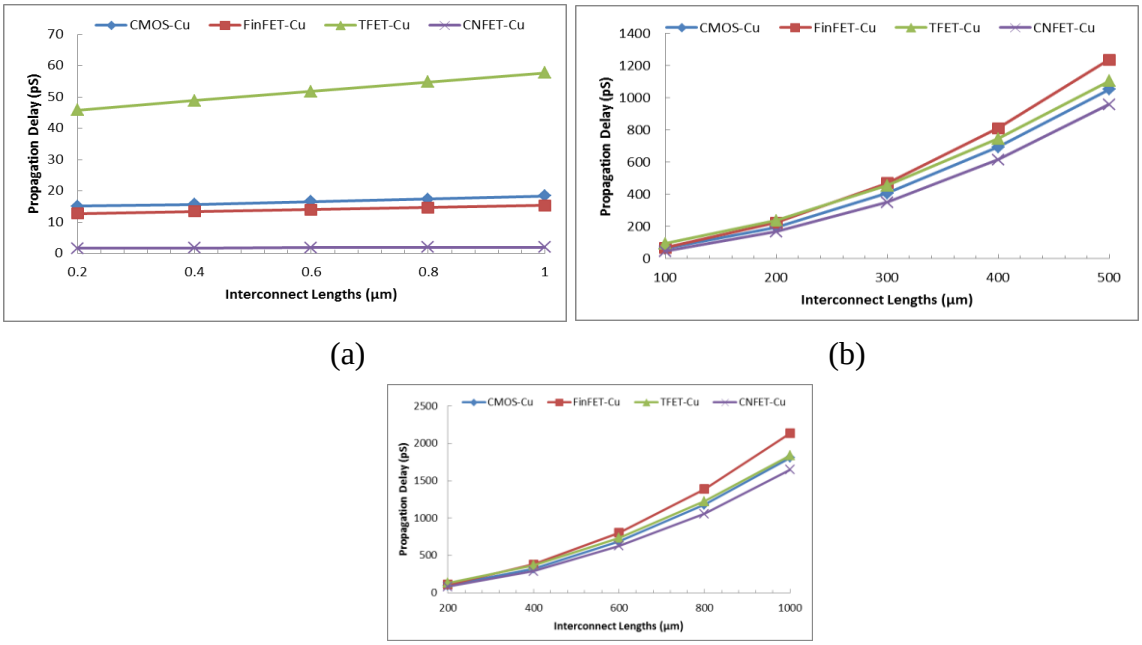
Figure 5.6: Test bench used for Cu interconnect incorporated with CMOS inverter driver.

The performance is analyzed in-terms of Pd, PD and PDP. There are two subsections namely interconnects and drivers. In interconnect subsection, interconnect material is common and drivers are varied to compare the performance of each interconnect with different interconnect drivers. Whereas in drivers subsection, driver is common and interconnect material are varied to compare the interconnect performance.

5.2.2 Performance analysis in terms of Propagation Delay

PD is one of the important parameter of consideration that measures the performance of interconnect. Following section shows PD as a function of interconnect lengths for Cu, SWCNT and MWCNTs.

A. Interconnects using Cu:

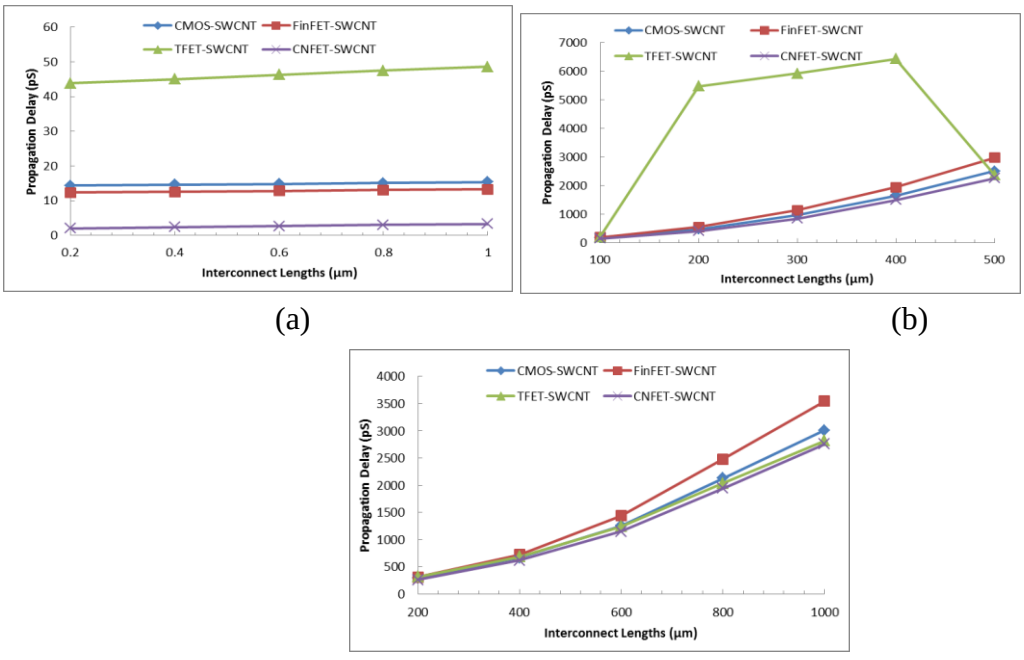


(a) (b)

(c)

Figure 5.7: PD of Cu interconnects incorporated with different drivers for various interconnect lengths.

B. Interconnects using SWCNT:

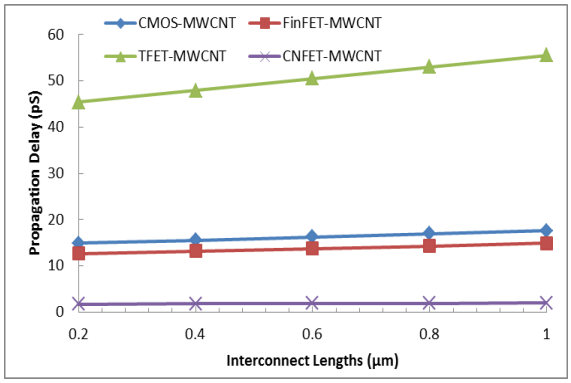


(a) (b)

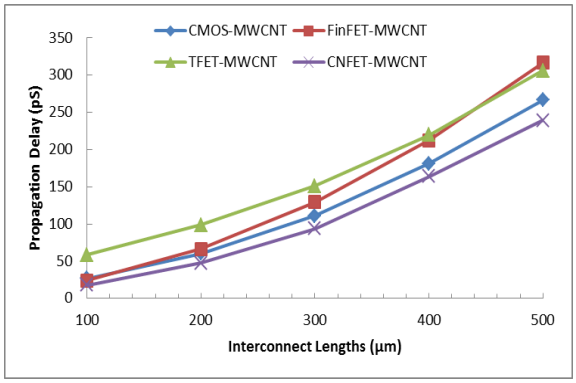
(c)

Figure 5.8: PD of SWCNT interconnects incorporated with different drivers for various interconnect lengths.

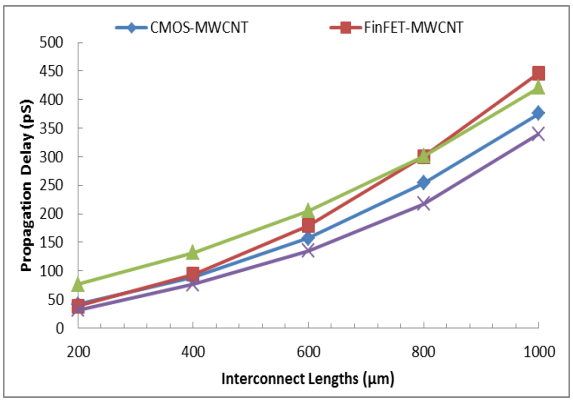
C. Interconnects using MWCNT:



(a)



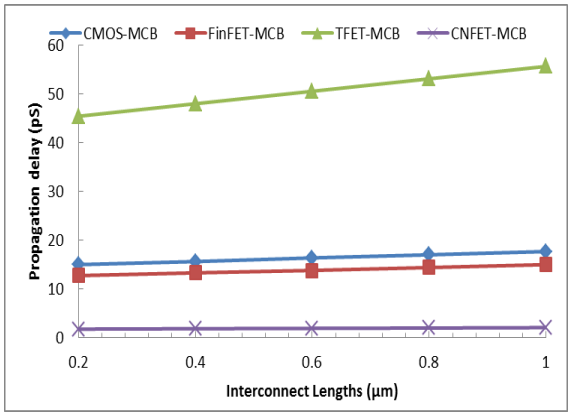
(b)



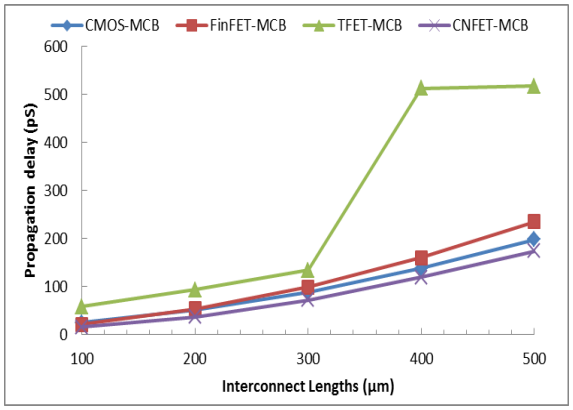
(c)

Figure 5.9: PD of MWCNT interconnects incorporated with different drivers for various interconnect lengths.

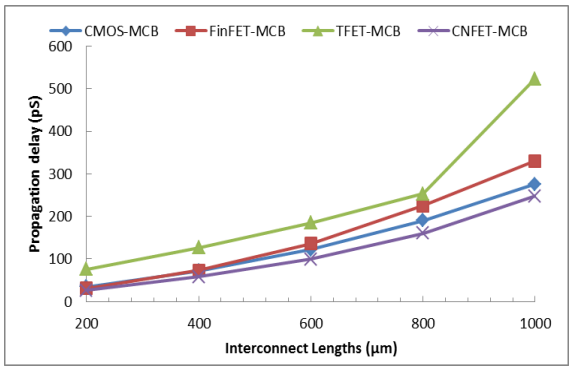
D. Interconnects using MCB:



(a)



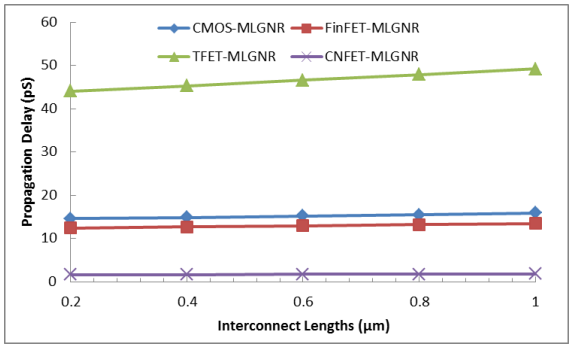
(b)



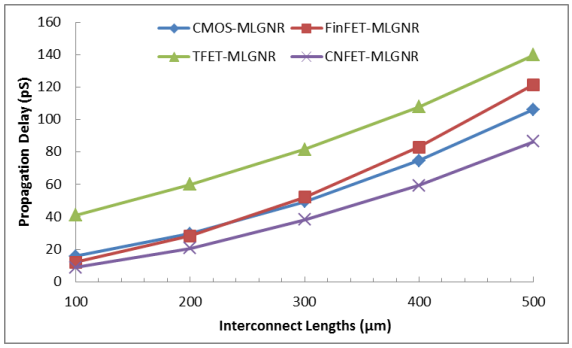
(c)

Figure 5.10: PD of MCB interconnects incorporated with different drivers for various interconnect lengths.

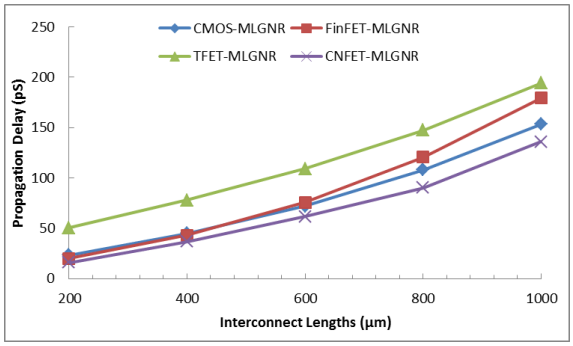
E. Interconnects using MLGNR:



(a)



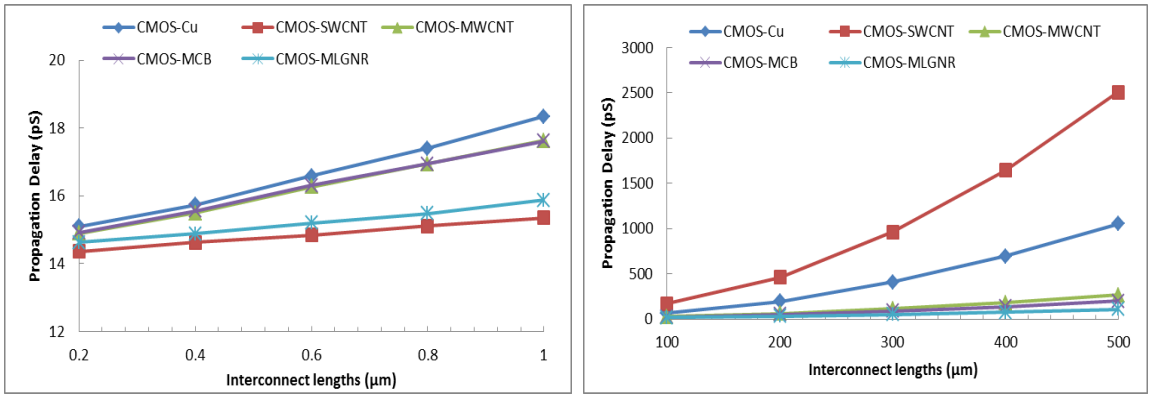
(b)



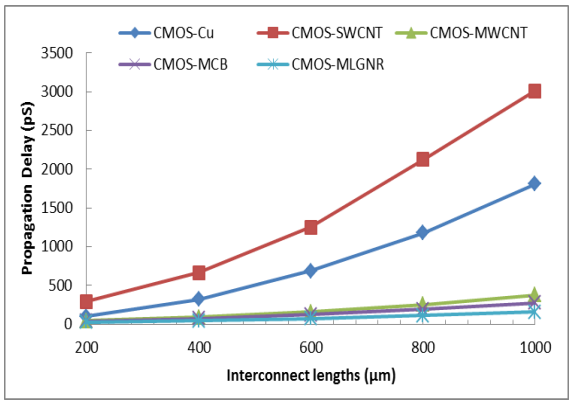
(c)

Figure 5.11: PD of MLGNR interconnects incorporated with different drivers for various interconnect lengths.

F. Drivers used considering CMOS:



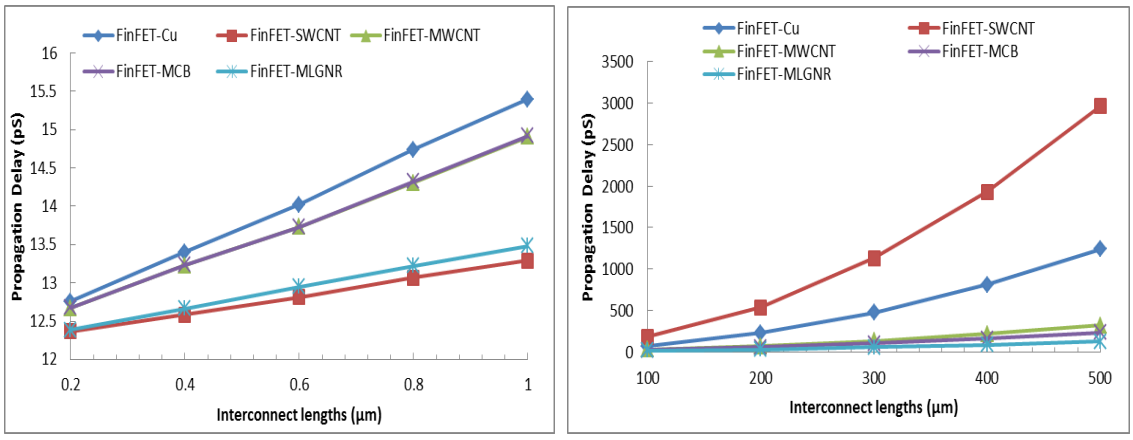
(a) (b)



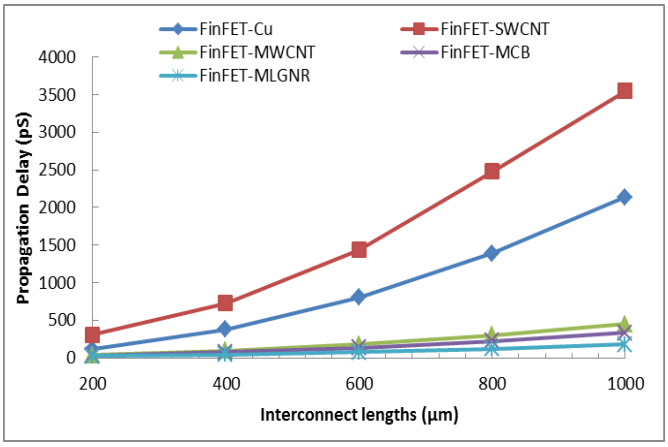
(c)

Figure 5.12: PD of different interconnects materials incorporated with CMOS driver for various interconnect lengths.

G. Drivers used considering FinFET:



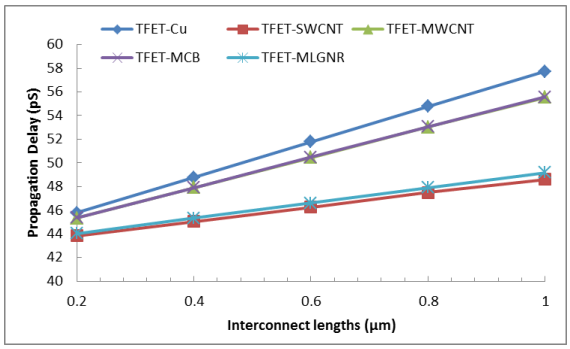
(a) (b)



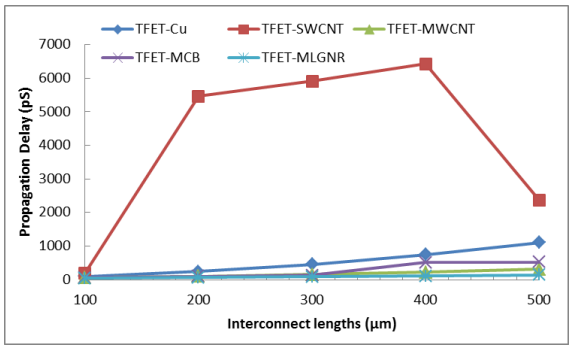
(c)

Figure 5.13: PD of different interconnects materials incorporated with FinFET driver for various interconnect lengths.

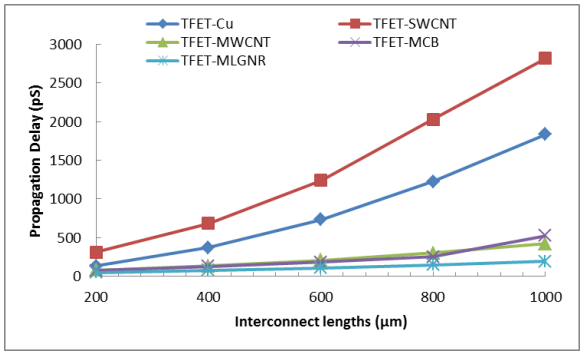
H. Drivers used considering TFET:



(a)



(b)



(c)

Figure 5.14: PD of different interconnects materials incorporated with TFET driver for various interconnect lengths.

I. Drivers used considering CNFET:

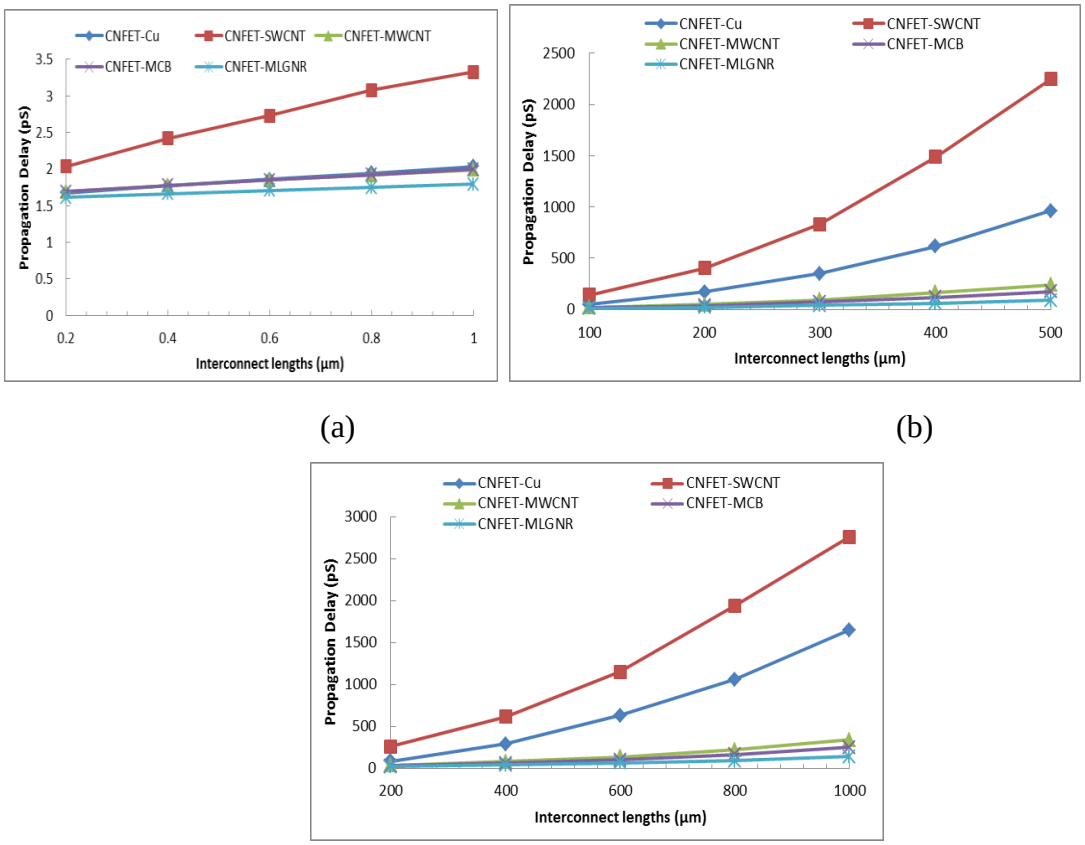
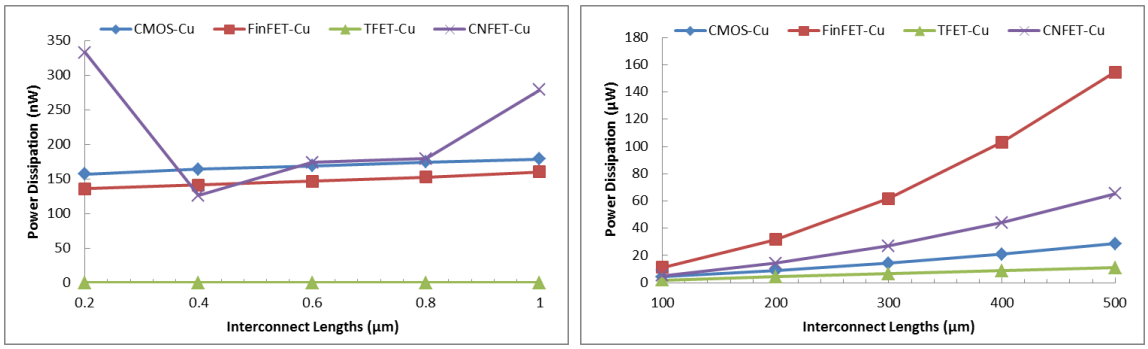


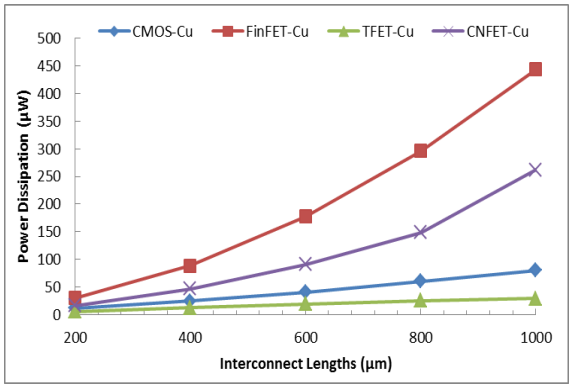
Figure 5.15: PD of different interconnects materials incorporated with CNFET driver for various interconnect lengths.

5.2.3 Performance analysis in terms of Power dissipation

Pd is the important parameter of consideration that measures the performance of interconnect. Following section shows Pd as a function of interconnect lengths.

A. Interconnects using Cu:

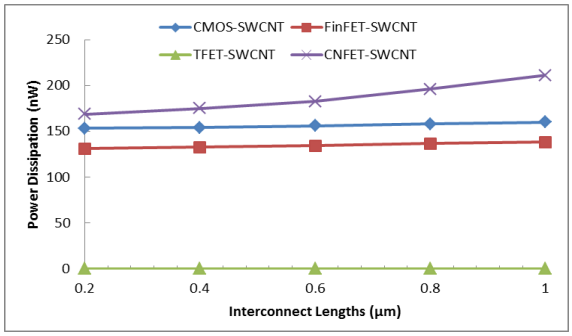




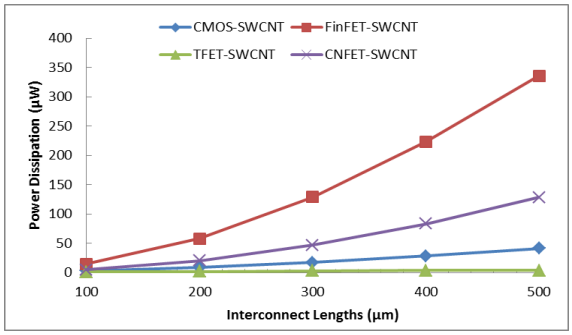
(c)

Figure 5.16: Pd of Cu interconnects incorporated with different drivers for various interconnect lengths.

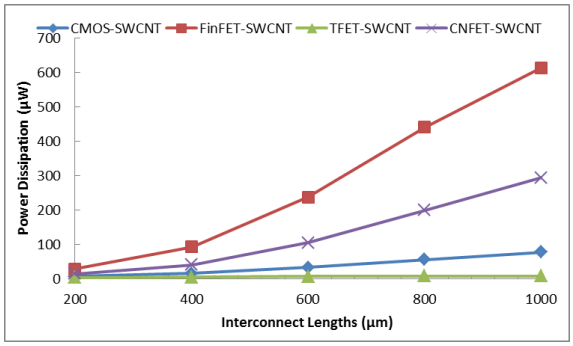
B. Interconnects using SWCNT:



(a)



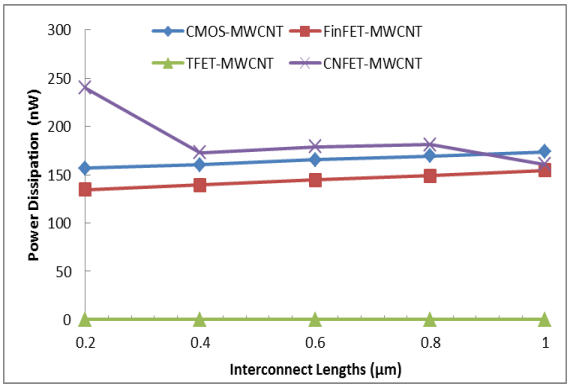
(b)



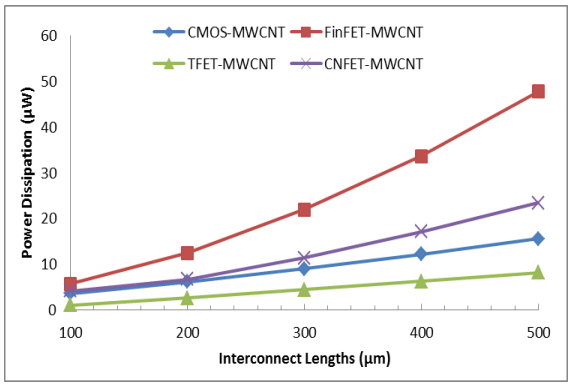
(c)

Figure 5.17: Pd of SWCNT interconnects incorporated with different drivers for various interconnect lengths.

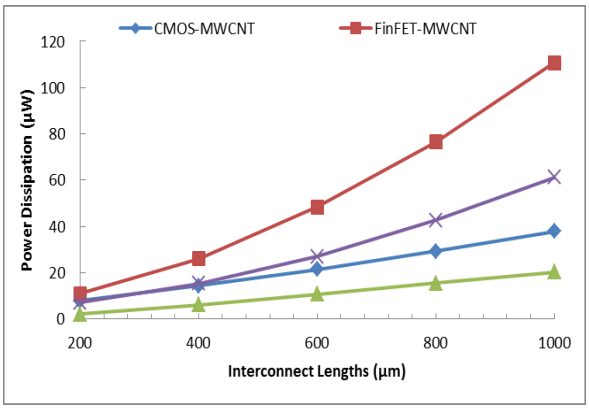
C. Interconnects using MWCNT:



(a)



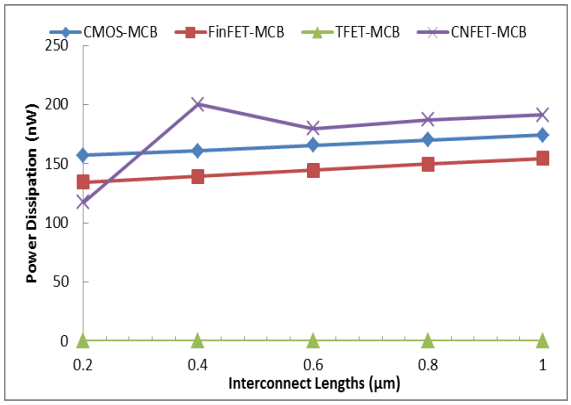
(b)



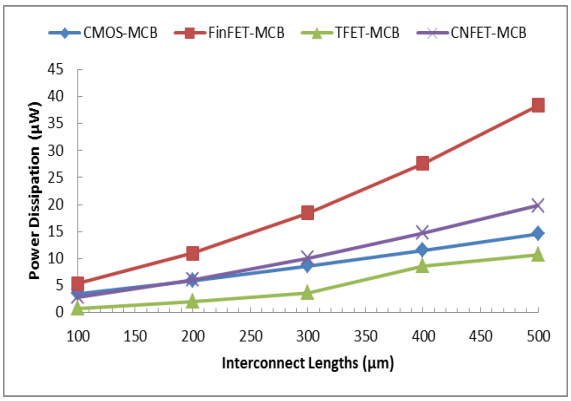
(c)

Figure 5.18: Pd of MWCNT interconnects incorporated with different drivers for various interconnect lengths.

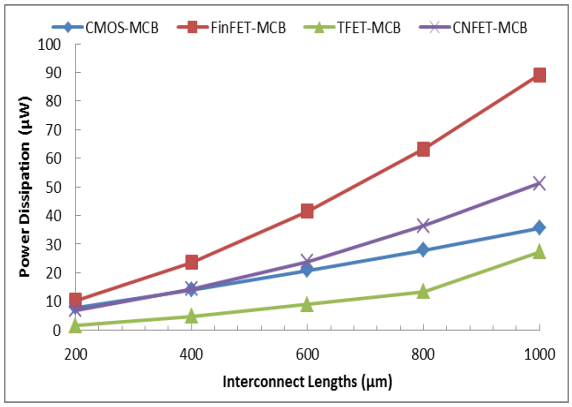
D. Interconnects using MCB:



(a)



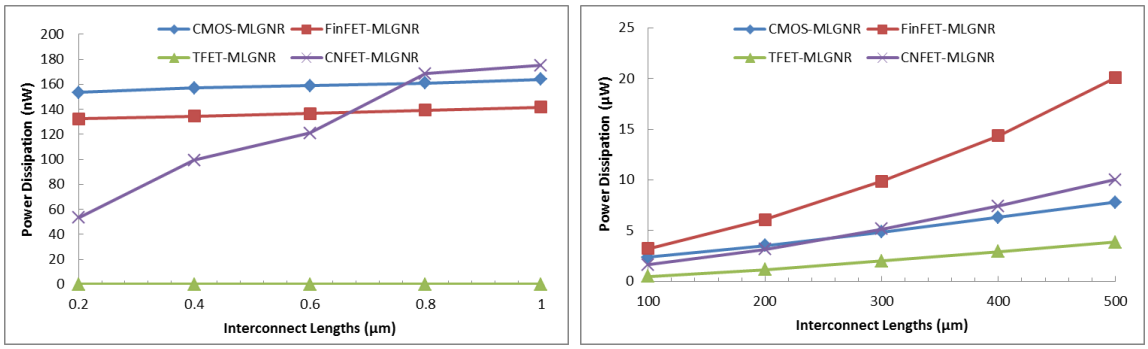
(b)



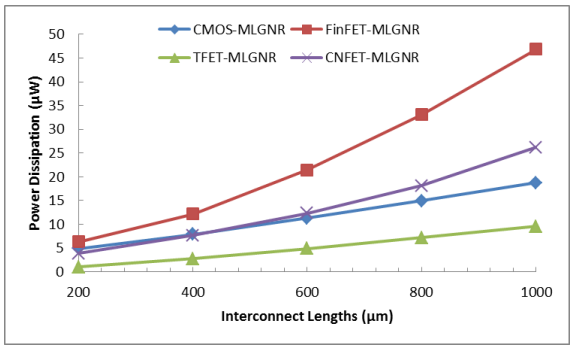
(c)

Figure 5.19: Pd of MCB interconnects incorporated with different drivers for various interconnect lengths.

E. Interconnects using MLGNR:



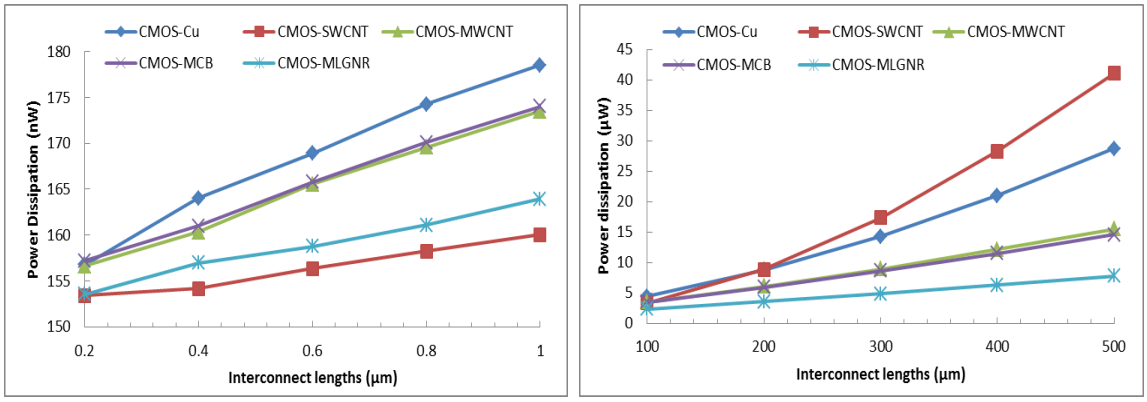
(a) (b)



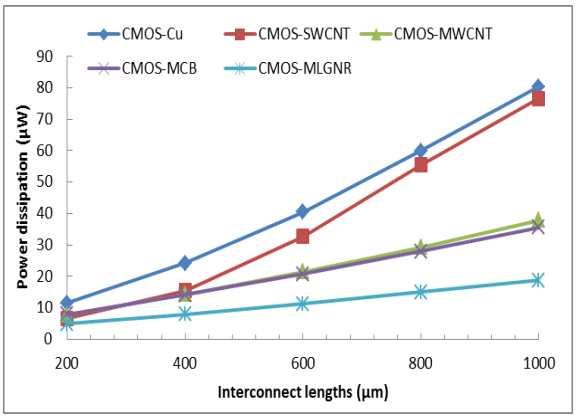
(c)

Figure 5.20: Pd of MLGNR interconnects incorporated with different drivers for various interconnect lengths.

F. Drivers using CMOS:



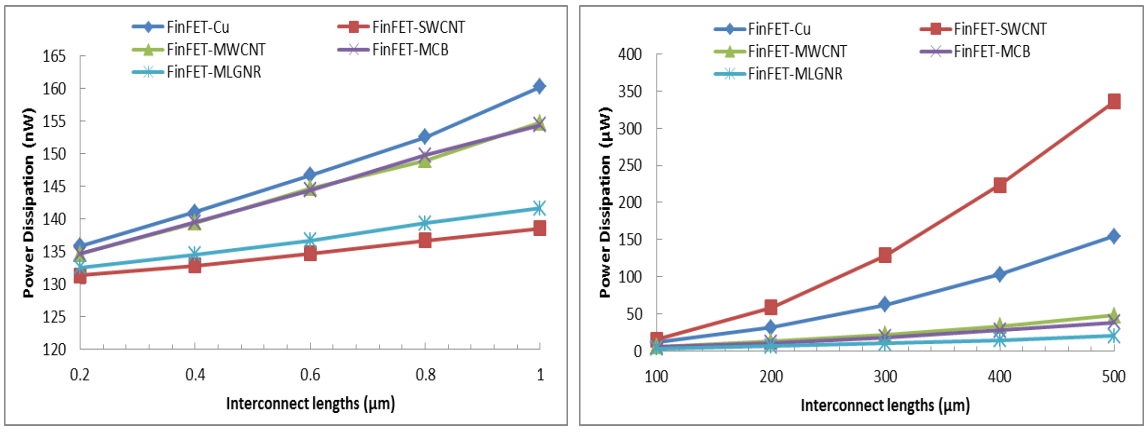
(a) (b)



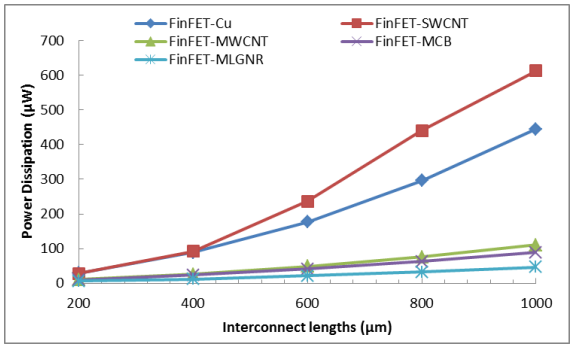
(c)

Figure 5.21: Pd of different interconnects materials incorporated with CMOS driver for various interconnect lengths.

G. Drivers using FinFET:



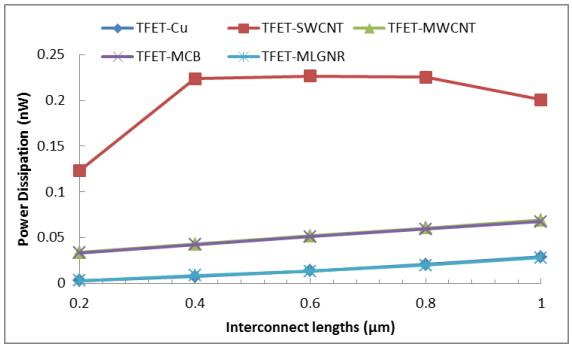
(a) (b)



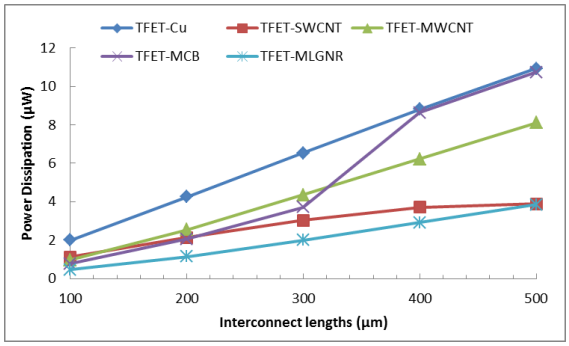
(c)

Figure 5.22: Pd of different interconnects materials incorporated with FinFET driver for various interconnect lengths.

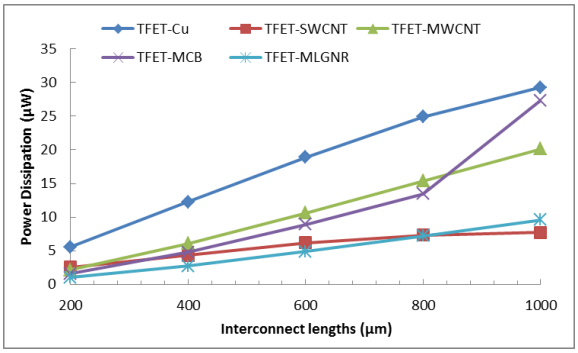
H. Drivers using TFET:



(a)



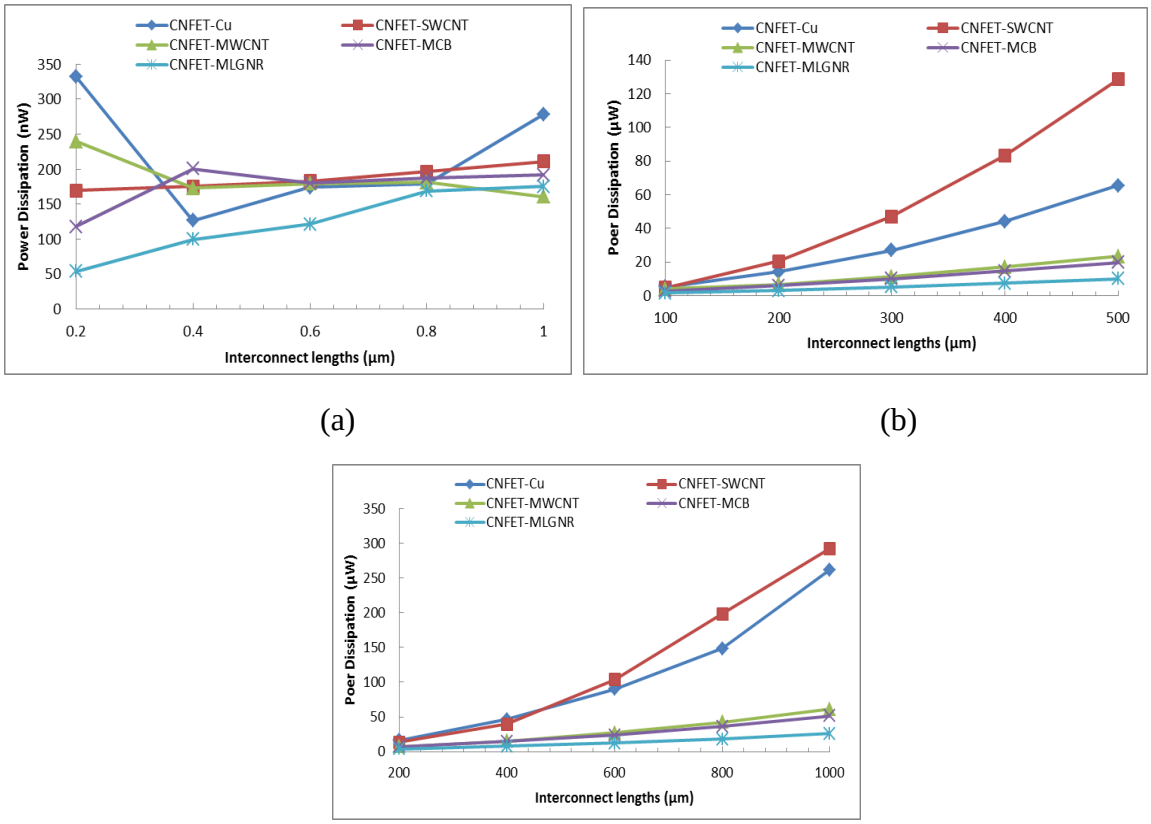
(b)



(c)

Figure 5.23: Pd of different interconnects materials incorporated with TFET driver for various interconnect lengths.

I. Drivers using CNFET:



(a) (b)

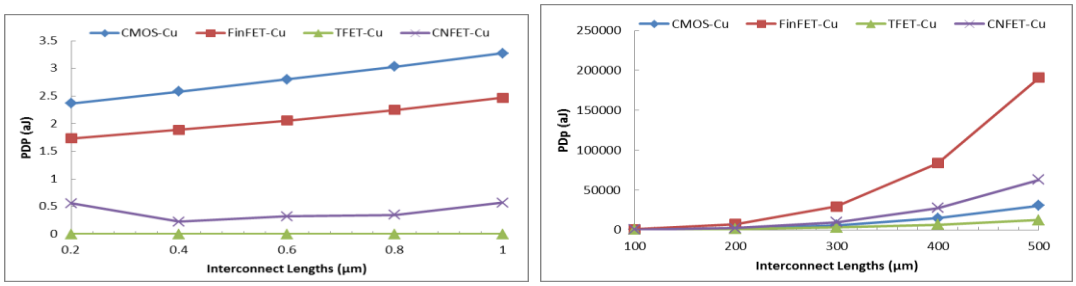
(c)

Figure 5.24: Pd of different interconnects materials incorporated with CNFET driver for various interconnect lengths.

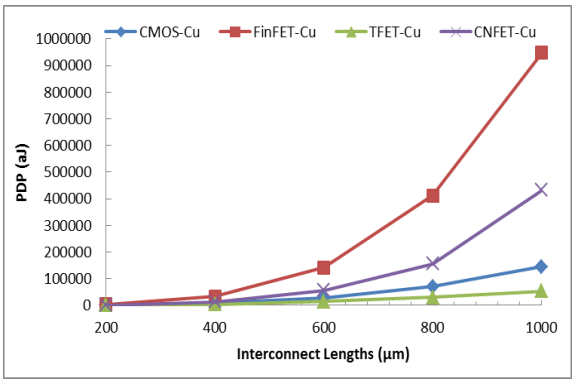
5.2.4 Performance analysis in terms of PDP

PDP is trade-off between Power and performance at given operation frequency. This section compared PDP of Cu, SWCNT and MWCNT interconnect with CMOS and FinFET driver for local, intermediate and global level interconnects.

A. Interconnects using Cu:



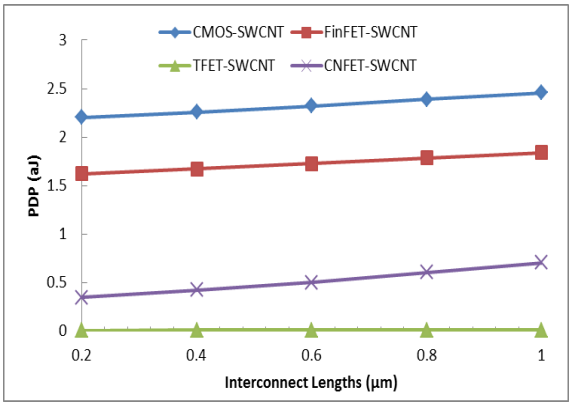
(a) (b)



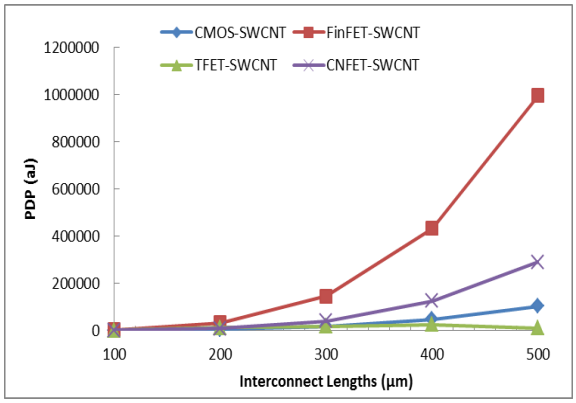
(c)

Figure 5.25: PDP of Cu interconnects incorporated with different drivers for various interconnect lengths.

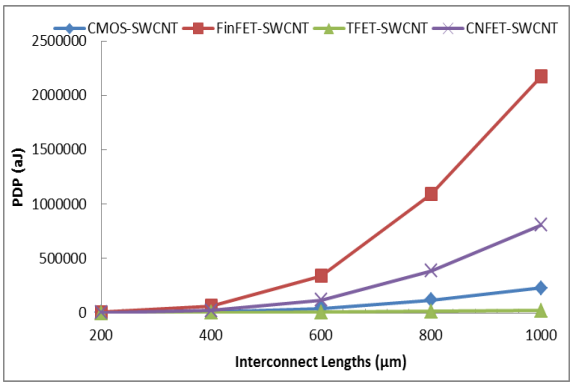
B. Interconnects using SWCNT:



(a)



(b)



(c)

Figure 5.26: PDP of SWCNT interconnects incorporated with different drivers for various interconnect lengths.

C. Interconnects using MWCNT:

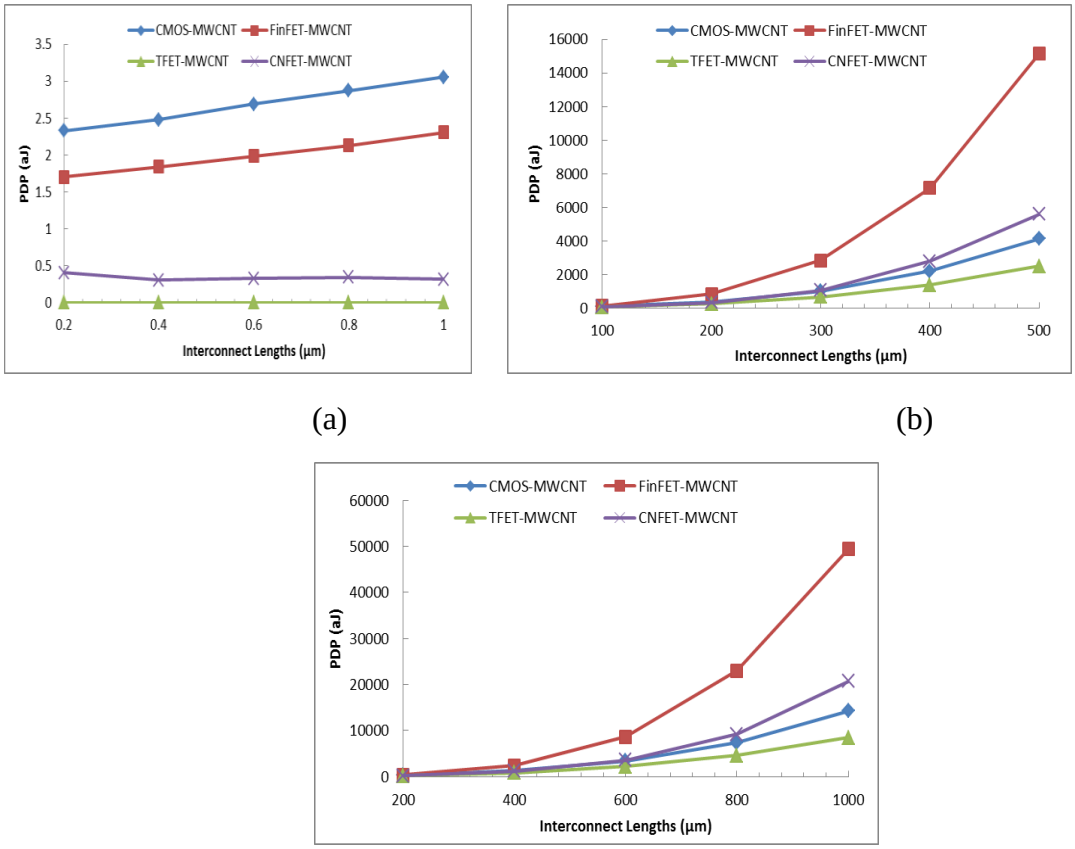
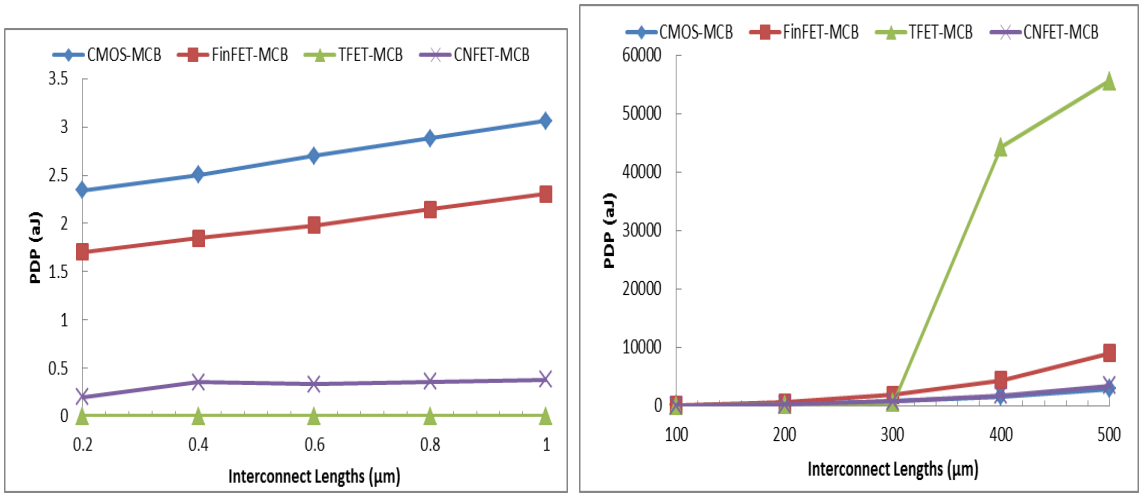
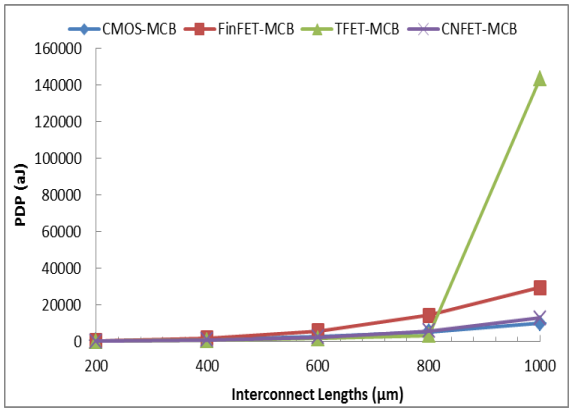


Figure 5.27: PDP of MWCNT interconnects incorporated with different drivers for various interconnect lengths.

D. Interconnects using MCB:

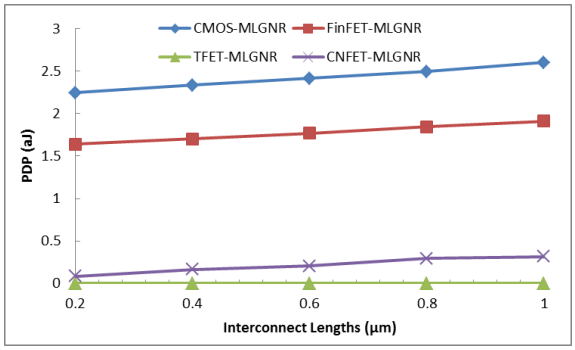




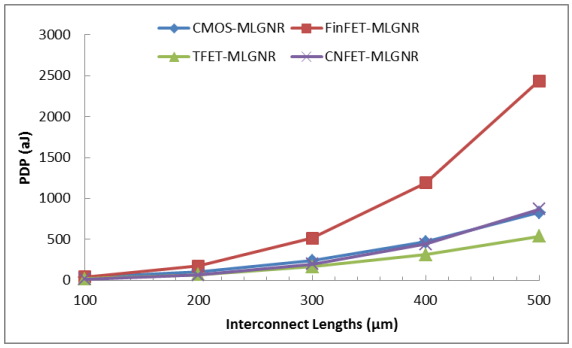
(c)

Figure 5.28: PDP of MCB interconnects incorporated with different drivers for various interconnect lengths.

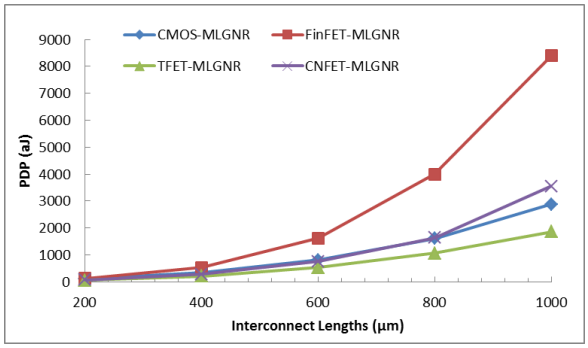
E. Interconnects using MLGNR:



(a)



(b)



(c)

Figure 5.29: PDP of MLGNR interconnects incorporated with different drivers for various interconnect lengths.

F. Drivers using CMOS:

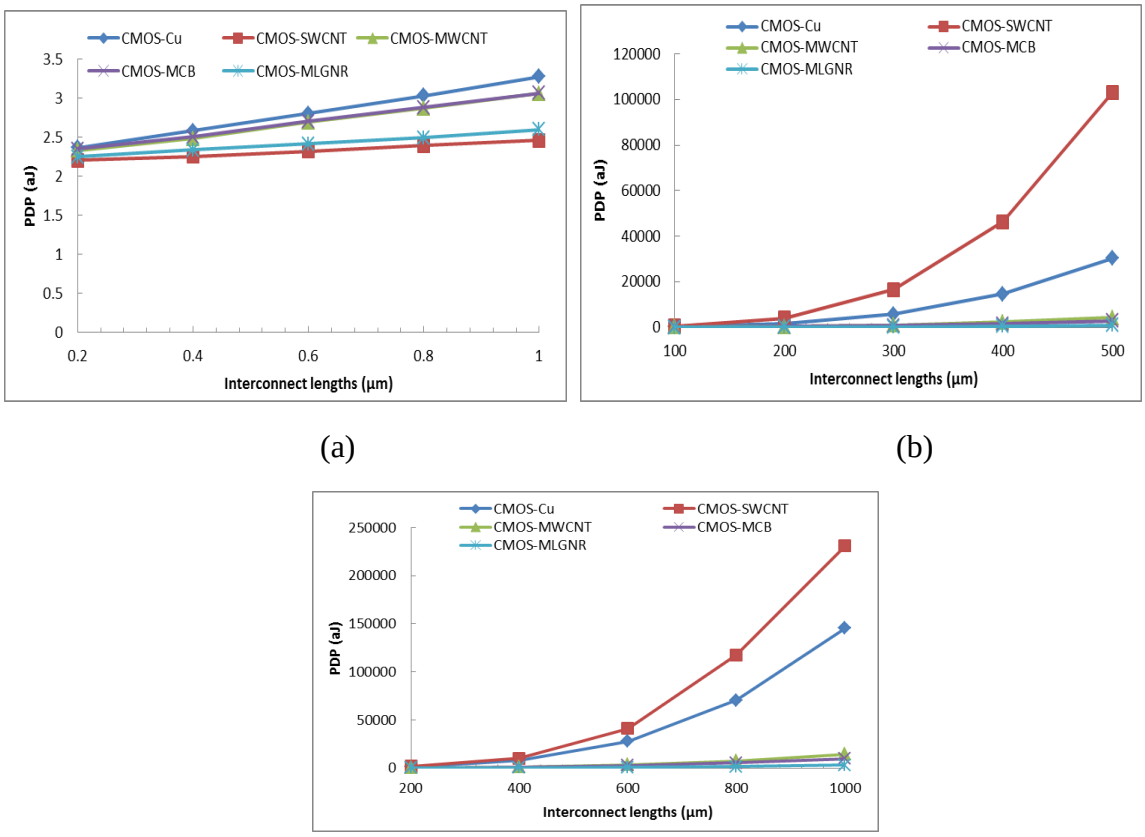
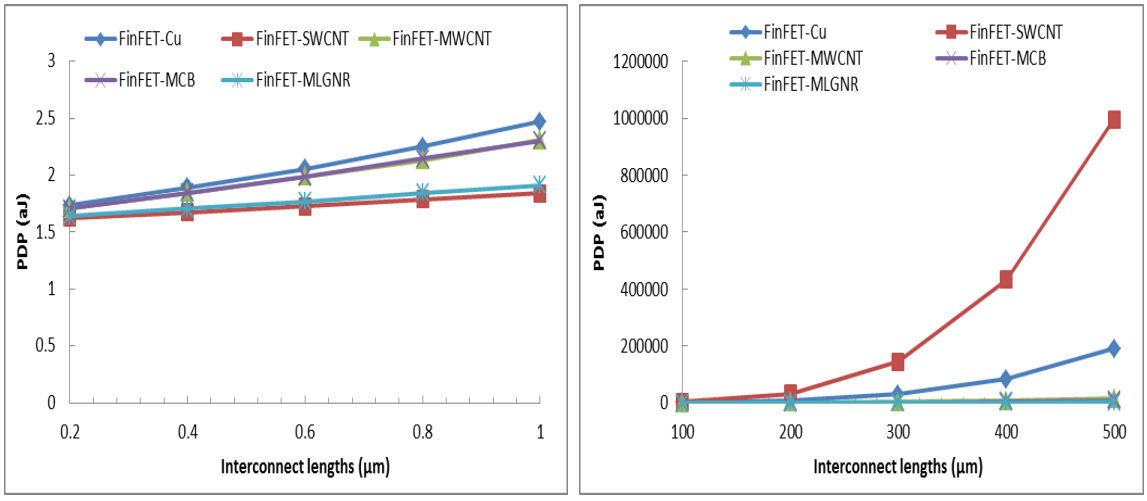
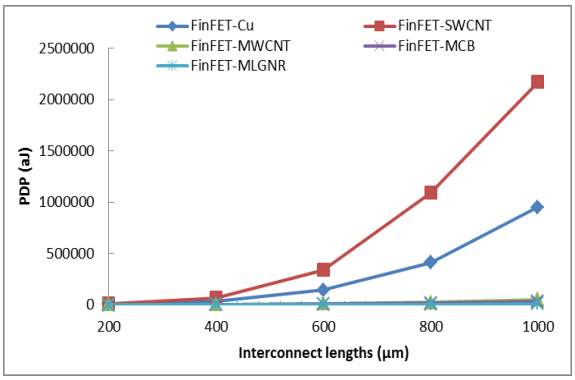


Figure 5.30: PDP of different interconnect materials incorporated with CMOS driver for various interconnect lengths.

G. Drivers using FinFET:

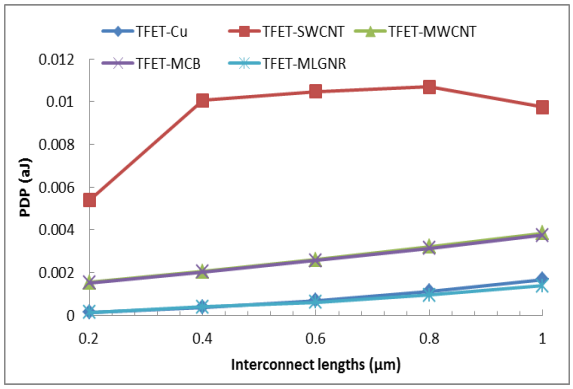




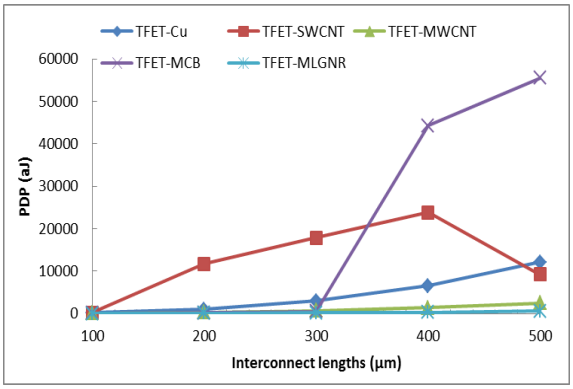
(c)

Figure 5.31: PDP of different interconnect materials incorporated with FinFET driver for various interconnect lengths.

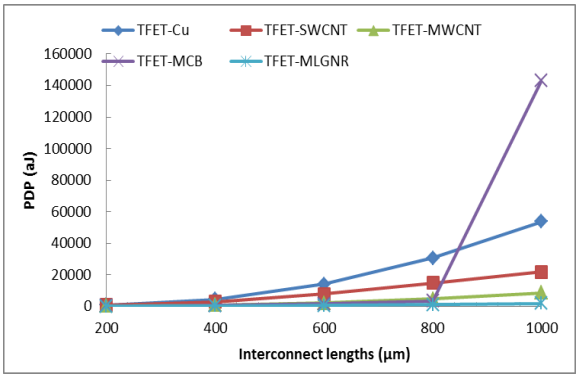
H. Drivers using TFET:



(a)



(b)



(c)

Figure 5.32: PDP of different interconnect materials incorporated with TFET driver for various interconnect lengths.

I. Drivers using CNFET:

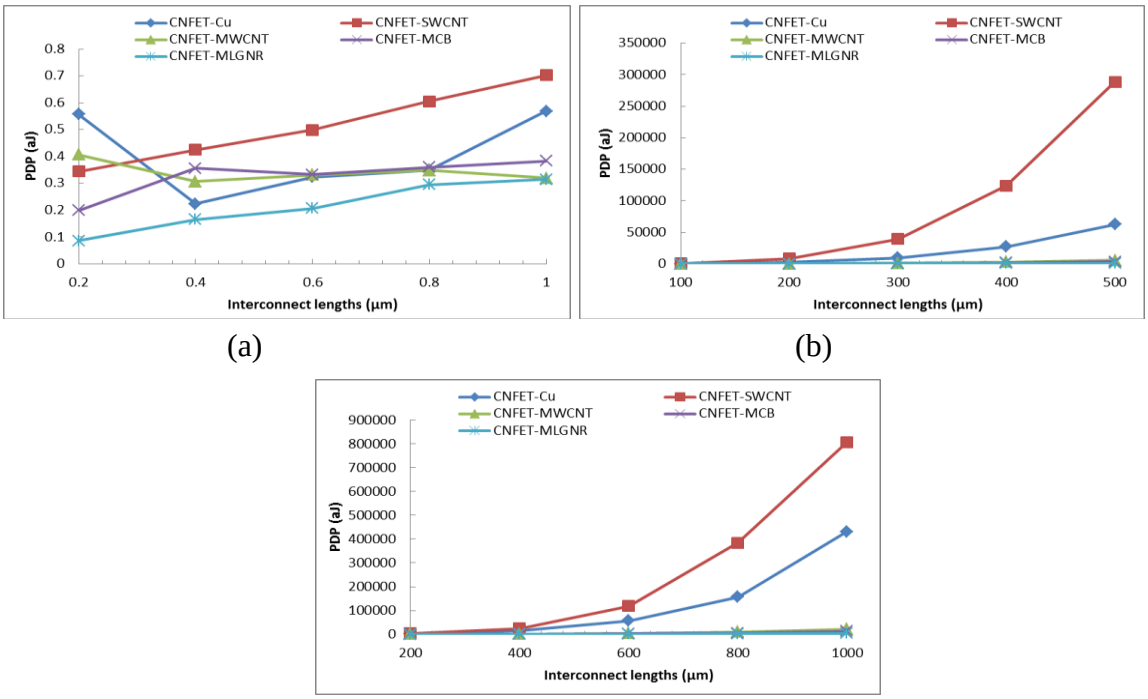


Figure 5.33: PDP of different interconnect materials incorporated with CNFET driver for various interconnect lengths.

5.2.5 Interpretation of Simulation Results

After analysing the simulation results for PD of Cu, SWCNT, MWCNT, MCB and MLGNR interconnects incorporated with CMOS, CNFET, FinFET and TFET driver for local, intermediate and global level are listed in Table 5.2 and PDP is listed in Table 5.3. From the Table 5.2 it is concluded that that propagation delay is little at local interconnects and it increments as the length of interconnection increments. for local lengths of interconnect, it has been shown that SWCNT has lower propagation delay than the Cu, MWCNT, MCB and MLGNR incorporated with CMOS, FinFET and TFET drivers. This is the fact that for smaller lengths, delay is influenced by capacitance of interconnect and SWCNT has lower capacitance which improves its performance at local level however utilizing CNFET driver MWCNT, MCB and MLGNR shows lower delay. While for intermediate and global lengths of interconnect, MWCNT, MCB and MLGNR has very low propagation delay as compared to Cu and SWCNT. This is on the grounds that delay is more influenced by resistance of interconnect for larger lengths and MWCNT, MCB and MLGNR offer less resistance contrasted with Cu and SWCNT. PDs

values for CMOS, CNFET, FinFET and TFET driver, shows that propagation delay is less for the CNFET driver than the remaining others. That means CNFET driver is able to drive interconnect efficiently than other devices. PDP is very less utilizing TFET driver compared to CMOS, FinFET and CNFET drivers.

- **AT LOCAL INTERCONNECT LEVEL (1µm) :** Considering CMOS driver, SWCNT interconnect shows reduction in propagation delay of 1.19X over Cu and 1.14X over MWCNT and MCB and 1.03X over MLGNR interconnect. Also SWCNT interconnect shows 1.33X, 1.24X and 1.06X reduction in PDP over Cu, MWCNT and MCB, and MLGNR respectively. Considering CNFET driver, MLGNR shows reduction in PD of 1.13X over Cu. Also MLGNR shows 1.8X reduction in PDP over Cu. Considering FinFET driver, SWCNT shows 1.15X reduction in PD and 1.33X reduction in PDP over Cu. Considering TFET driver, SWCNT shows 1.18X and 1.21X reduction in PD and PDP respectively over Cu. Additionally Cu interconnect with CNFET driver shows 9X reduction in PD over Cu interconnect with CMOS driver.
- **AT INTERMEDIATE INTERCONNECT LEVEL (500µM):** For Intermediate level interconnects, utilizing CMOS driver, MLGNR interconnect shows 9.93X and 36.56 X reductions in PD and PDP respectively over Cu interconnect. Considering CNFET driver, MLGNR interconnect shows 11.09X reduction in PD and 72.48X reduction in PDP. Considering FinFET driver, MLGNR interconnect shows 10.19X and 78.36X reduction in PD and PDP respectively over Cu. Utilizing TFET driver, MLGNR interconnect shows 7.91X reduction in PD and 22.47X reduction in PDP. Additionally Cu interconnects with CNFET driver shows 1.09X reduction in PD over Cu interconnect with CMOS driver.
- **AT GLOBAL INTERCONNECT LEVEL (1000 µM) :** Considering CMOS driver, MLGNR interconnect shows 11.79X and 50.4X reductions in PD and PDP respectively over Cu interconnect. Considering CNFET driver, MLGNR interconnect shows 12.14X reduction in PD and 124.8X reduction in PDP. Considering FinFET driver, MLGNR interconnect shows 11.90X and 112.9X reduction in PD and PDP respectively over Cu. Utilizing TFET driver, MLGNR interconnect shows 9.47X reduction in PD and 28.98X reduction in PDP. Additionally Cu interconnects with CNFET driver shows 1.09X reduction in PD over Cu interconnect with CMOS driver.

Table 5.2: PD of Cu, SWCNT, MWCNT, MCB and MLGNR incorporated with CMOS, CNFET, FinFET and TFET for various interconnect lengths at 32nm node.

Wire Length (µm)	Propagation Delay (pS)																			
	CMOS					CNFET					FinFET					TFET				
	Cu	SWCNT	MWCNT	MCB	MLGNR	Cu	SWCNT	MWCNT	MCB	MLGNR	Cu	SWCNT	MWCNT	MCB	MLGNR	Cu	SWCNT	MWCNT	MCB	MLGNR
Local																				
0.2	15.09	14.36	14.89	14.92	14.63	1.67	2.03	1.69	1.69	1.61	12.76	12.36	12.67	12.67	12.38	45.77	43.84	45.34	45.35	44.04
0.4	15.74	14.63	15.49	15.55	14.88	1.77	2.41	1.77	1.77	1.66	13.40	12.58	13.23	13.23	12.66	48.78	45.03	47.90	47.92	45.32
0.6	16.59	14.84	16.26	16.30	15.19	1.86	2.72	1.84	1.85	1.70	14.01	12.81	13.73	13.73	12.95	51.78	46.26	50.46	50.48	46.61
0.8	17.40	15.11	16.94	16.94	15.48	1.94	3.08	1.92	1.92	1.75	14.74	13.07	14.30	14.32	13.22	54.76	47.50	53.01	53.04	47.89
1	18.34	15.35	17.63	17.61	15.87	2.03	3.32	1.99	1.99	1.79	15.39	13.29	14.90	14.92	13.48	57.72	48.60	55.55	55.58	49.17
Intermediate																				
100	64.11	168.39	26.42	24.30	15.85	47.51	141.11	17.51	14.57	8.70	68.90	180.1	24.00	20.20	12.09	94.47	194.79	58.48	57.55	41.10
200	195.53	461.58	59.85	50.48	29.74	168.33	403.08	47.30	36.03	20.52	225.85	537.46	66.25	52.42	28.19	237.33	5463.9	98.59	92.63	59.97
300	408.01	960.58	110.85	87.07	49.29	349.95	832.74	93.40	71.35	38.13	471.3	1128	129.13	98.39	52.06	455.8	5913.3	150.89	133.35	81.56
400	693.38	1641.8	181.42	136.77	74.74	615.31	1489.1	163.77	118.37	59.33	811.4	1930	212.16	159.02	82.89	745.67	6424.8	219.76	511.81	107.75
500	1053.3	2504.7	266.43	197.12	106.05	960.33	2248.2	239.34	173.24	86.52	1237.2	2963.6	316.8	234.35	121.4	1105.6	2366.4	305.91	517.07	139.76
Global																				
200	98.26	288.35	41.35	34.82	23.25	81.64	256.59	31.17	26.24	16.04	110.47	304.31	38.53	31.12	19.99	133.98	311.16	75.96	75.75	50.45
400	321.89	662.36	89.21	72.11	44.72	289.67	613.75	76.09	58.28	36.83	379.32	722.57	93.46	73.32	43.14	369.68	682.06	132.1	127.06	78.05
600	683.95	1251.6	156.91	121.56	72.04	627.35	1146.8	134.59	99.28	61.61	803.45	1435.6	179.15	135.93	75.67	735.59	1239.2	204.98	184.44	109.12
800	1178	2124.4	253.64	190.42	107.87	1057.1	1940.7	217.18	160.62	89.99	1389.7	2477	300.4	225.17	120.68	1225.6	2031.6	300.59	253.48	147.23
1000	1809.3	3011.5	375.28	275.78	153.41	1647.4	2758.8	339.46	247.97	135.67	2134.9	3545.5	446.32	330.36	179.4	1837.8	2819.5	421.28	523.28	194

Table 5.3: PDP of Cu, SWCNT, MWCNT, MCB and MLGNR incorporated with CMOS, CNFET, FinFET and TFET for various interconnect lengths at 32nm node.

Wire Length (µm)	Power Delay Product (aJ)																			
	CMOS					CNFET					FinFET					TFET				
	Cu	SWCNT	MWCNT	MCB	MLGNR	Cu	SWCNT	MWCNT	MCB	MLGNR	Cu	SWCNT	MWCNT	MCB	MLGNR	Cu	SWCNT	MWCNT	MCB	MLGNR
Local																				
0.2	2.366896	2.20388806	2.3329961	2.3457463	2.2465900	0.5573895	0.3440874	0.40604763	0.19915458	0.08609658	1.733063	1.6237871	1.7051443	1.70541344	1.64100384	0.00013931	0.00539198	0.001528	0.00152027	0.00013742
0.4	2.5816814	2.25595389	2.4835117	2.5041994	2.3369774	0.2238264	0.4239279	0.30647198	0.35563074	0.16503526	1.890225	1.6707637	1.8437398	1.8454884	1.70407575	0.00036827	0.01006465	0.002046	0.00202335	0.00039750
0.6	2.8025487	2.32178176	2.6931674	2.7025483	2.4129932	0.3238265	0.4986685	0.33097622	0.3325375	0.20630091	2.055739	1.7252769	1.9868830	1.98248884	1.7693585	0.00069493	0.01047694	0.002611	0.00256893	0.00061168
0.8	3.0331691	2.3908553	2.8723464	2.8814960	2.4944661	0.3494229	0.6045679	0.34774603	0.3596613	0.29497805	2.249039	1.7857541	2.1310335	2.14545525	1.84263925	0.00112505	0.01069625	0.003211	0.00314344	0.00095402
1	3.2754899	2.4580479	3.0593311	3.0653665	2.6014104	0.5679980	0.7026143	0.31996063	0.38225152	0.31439891	2.466894	1.8409308	2.3068582	2.3038024	1.9097457	0.00166608	0.00974461	0.003838	0.00374756	0.00137038
Intermediate																				
100	281.93691	563.635008	92.36074	85.046399	37.490785	246.04996	686.86703	71.838277	41.7254136	14.182793	770.0580	2705.2821	134.23671	107.746304	38.9027925	189.161849	220.015305	56.89362	44.5161126	18.8856922
200	1716.1472	4095.46086	362.6497	300.12591	105.10619	2405.6040	8246.2106	313.912234	218.962152	64.6753734	7169.156	31316.181	823.61590	577.566225	171.510628	1012.68711	11708.0449	250.9535	191.124532	68.5322898
300	5843.1112	16667.0235	990.4558	752.61560	238.96260	9465.4476	39234.545	1055.81620	718.728696	196.427095	29180.53	145252.56	2830.0130	1815.89818	513.304735	2979.06322	17894.2371	656.7939	494.7285	162.783435
400	14557.513	46426.8204	2197.359	1576.0007	470.16610	27143.170	124129.88	2786.05524	1745.36565	440.160381	83777.05	431702.4	7132.3948	4390.5422	1189.26587	6570.09837	23861.7072	1367.456	44249.0453	313.929625
500	30261.309	103003.282	4132.062	2871.2499	827.62480	62779.653	288781.29	5580.2121	3433.44356	866.161731	191011.3	995325.06	15140.188	8983.5729	2437.4692	12094.1584	9211.92192	2479.798	55538.4887	538.173832
Global																				
200	1124.8165	1891.37415	323.5215	273.458121	113.576719	1320.77192	3424.19355	220.212504	182.102976	62.386169	3295.2096	8604.36525	418.58992	323.430216	125.591720	742.624344	791.030952	162.15061	120.686493	49.6200720
400	7794.8882	10168.5507	1273.333	1015.1769	354.85853	13394.630	24241.283	1162.35084	833.549164	281.460192	33615.338	66532.077	2424.1914	1730.962168	526.424346	4519.70768	2933.54006	801.93947	607.003738	212.069655
600	27671.2491	40899.7848	3366.347	2522.8562	813.55901	56591.988	118774.07	3633.79541	2367.62944	759.67596	142483.82	339964.43	8667.4561	5647.21185	1624.601093	13900.44423	7656.02544	2174.8378	1642.825524	531.654464
800	70516.258	117647.147	7395.127	5315.1934	1608.9889	156704.50	385073.69	9243.1808	5842.5525	1629.053286	411656.93	1090647.8	22972.489	14246.95624	3994.99072	30555.4336	14868.46776	4617.9641	3408.79904	1056.993616
1000	145268.697	230909.774	14226.864	9821.3531	2881.3466	431767.06	807969.75	20733.53788	12700.77543	3548.58452	948600.1	2171760.57	49398.6976	29448.62076	8400.0462	53788.7304	21786.8404	8493.0048	143122.3128	1855.4548

5.3 Summary

Due to technology scaling, CMOS performance is improved but leakage currents and power consumption is increased also interconnect performance has been degraded. Cu interconnects has been used since many decades until the problem aroused while technology reaches 45nm. Hence new interconnect material such as CNT and GNR comes into consideration. Therefore, in this work performance of conventional Cu and these emerging interconnect is analyzed with the CMOS, FinFET, TFET, and CNFET device technology.

Performance analysed of Cu, SWCNT, MWCNT, MCB and MLGNR interconnect incorporated with CMOS, CNFET, FinFET and TFET driver for local, intermediate and global level interconnect is carried out. Postponement is to a great extent affected by interconnect capacitance at nearby level thus SWCNT performs better which has low capacitance esteem though delay is to a great extent affected by interconnect protection at middle of the road and worldwide level subsequently MWCNT, MCB and MLGNR performs better which has low resistance esteems. Therefore, SWCNT is conceivable possibility for supplanting Cu at local level likewise MWCNT, MCB and MLGNR for intermediate and global level for CMOS, FinFET and TFET devices. However, utilizing CNFET driver MCB, MWCNT and MLGNR are appropriate for all level of interconnects compared to Cu interconnect technology.

Next Chapter deals with the performance evaluation of the circuit level simulations executed on the different building blocks of FPGA.

Chapter 6

PERFORMANCE EVALUATION OF CIRCUIT LEVEL SCHEMATICS

The different types of the schematics which make a vital performance in the operation of the FGPA for different applications are based on the circuit performance of the different building block of the FPGA. These circuits are herewith elaborated in terms of the performance analysis.

6.1 Digital Circuits:

6.1.1 Analysis of 6T SRAM Cell:

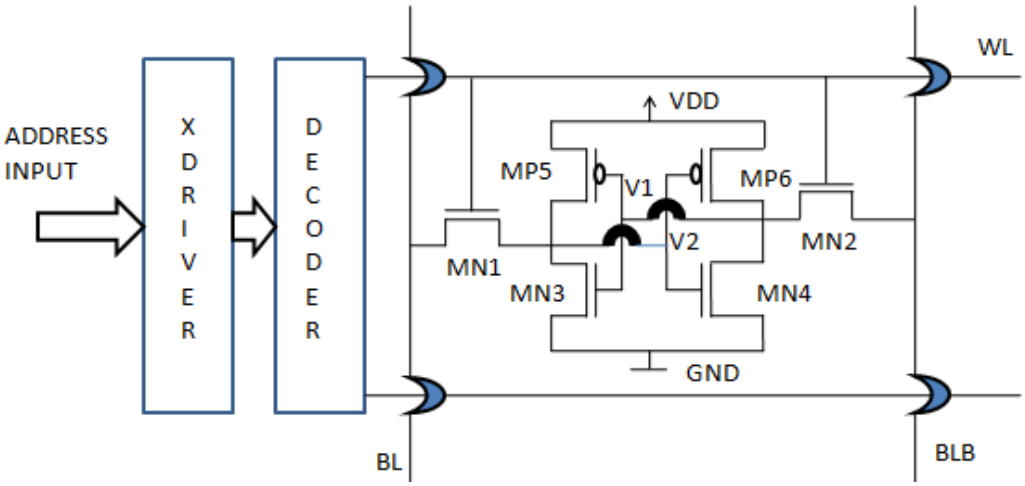


Figure 6.1: Design of 6T SRAM Cell.

The discharging strength of the access transistor must overcome the restoring strength of the pull-up transistor. The pull up ratio, which is the ratio of the strength of the pass-gate transistor to that of the pull-up transistor should be sufficiently large to ensure that write failure does not occur.

1. **Pull up ratio (PR):** It is ratio of PMOS from the inverter to the MN1 access transistor right side
2. **Cell up ratio (CR):** It is ratio of the NMOS of the inverter and the access transistor MN2 right side

$$PR = \frac{W_6 L_2}{L_6 W_2} \quad \text{.....(6.1)}$$

$$CR = \frac{W_3 L_1}{L_3 W_1} \quad \text{.....(6.2)}$$

Proper '*W/L'* ratio is to be design for getting good stability in all modes (read, write, hold)

Transistor Sizing of CNFET based 6T SRAM CELL:

The Transistor sizing of CNFET based 6T SRAM cell is given below:

Table 6.1: Transistor sizing of CNFET Based 6T SRAM Cell.

No of Transistor	Number of Tubes
Pull up Transistor	2
Pull down Transistor	10
Access Transistor	5

Table 6.2: Design of double gate CNFET

Cell Ratio	Pull up Ratio
2	0.4

Now as per the theoretical details of the SRAM and CNFET transistor, a 32nm device is designed and simulated in the HSPICE and by using its parameters the 6T SRAM cell is designed and compared their parameters with the conventional MOSFET. SRAM is designed using the inverter, so here is the simulation result and comparison of the transistors.

Two cross coupled inverter having transistor inverter 1 (MP5-PMOS & MN3-NMOS) inverter 2 (MP6-PMOS & MN4-NMOS) and two access transistor MN1 (NMOS) and MN2 (NMOS) these transistor enable access to the cell during read and write operation. When world line is activating the two access transistor MN3 and MN4 are connected to the internal node of the cell to the BL and BLB line [120].

Table 6.3: Operation of the 6T SRAM.

	Read	Write	Hold
BL	Logic 1	Logic 0	Logic 0
BLB	Logic 0	Logic 1	Logic 0
WL	Logic 1	Logic 1	Logic 0

Read Operation

During scan operation WL is activated and also the BL is pre charge to V_{DD} and BLB is store to zero [121]. The voltage at BL is remaining at the pre charge level and also the voltage at BLB discharges through MN2 serial with MN4 electronic transistor.

Write Operation

During the write operation, the bit-lines are driven to complementary voltage levels via a write driver then the word-line is chosen [122]. On the facet of the cell that the bit-line voltage is logic '0' (i.e., an occasional voltage), the interior storage node is discharged through the access electronic transistor [123].

Pull up and Cell ratio

1) **Pull up ratio (PR):** It is ratio of PMOS of the inverter to the MN1 access transistor right side
2) **Cell up ratio (CR):** It is ratio of the NMOS of the inverter and the access transistor MN2 right side

$$PR = \frac{W_6 L_2}{L_6 W_2} \quad \text{.....(6.3)}$$

$$CR = \frac{W_3 L_1}{L_3 W_1} \quad \text{.....(6.4)}$$

Proper W/L ratio is to be design for getting good stability in all modes (read, write, hold).

Simulation Results

Select a proper transistor and improve the parameters of the SRAM cell is which plays a major role in designing a SRAM.

MOSFET Inverter

Using 32 nm CMOS technology CMOS inverter is simulated and obtained the following waveform.

Table 6.4: Output voltage of the CMOS inverter.

Input Voltage	Output Voltage
0.00V	2.22V
3.00V	0.01V

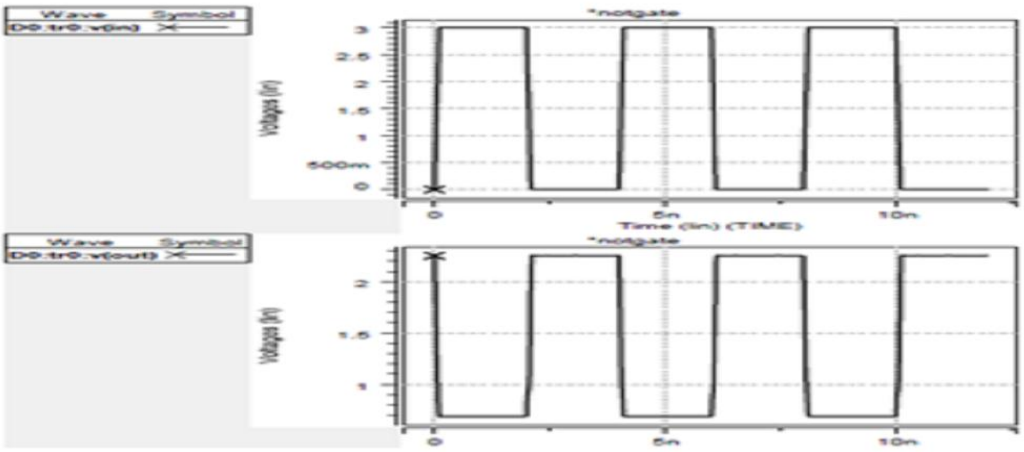


Figure 6.2: CMOS inverter output waveform.

CNFET Inverter

CNFET inverter is simulated in the HSPICE, we obtained better result as compared to TFET invertor and the same are reported in below waveforms.

Table 6.5: Output voltage of the CNFET inverter.

Input Voltage	Output Voltage
0.00V	2.22V
3.00V	0.01V

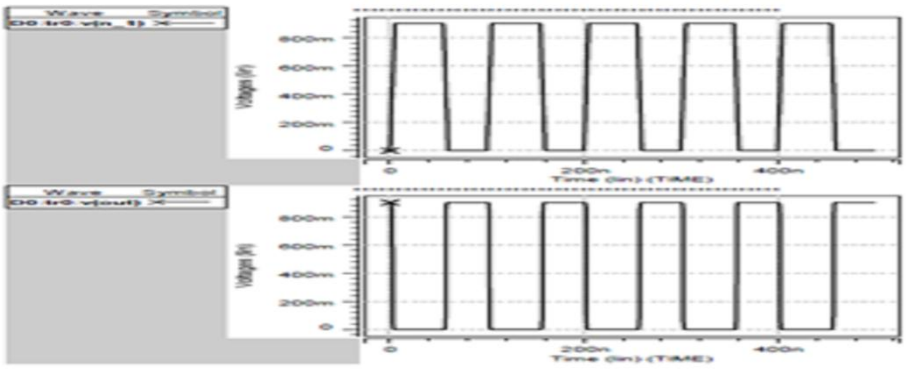


Figure 6.3: CNFET inverter output waveform.

Comparison and analysis of the CMOS and CNFET inverter

Table 6.6: Comparison CNFET and CMOS inverter.

Applied Voltage	MOSFET	CNFET
0.00V	2.22V	3.00V
3.00V	0.01V	0.00V

CNFET simulation of SRAM

The Transistors required for design of a 6T SRAM cell is required to be selected such that it improve the various performance parameters. After selection of proper transistor, sizing plays an important role in the improvement of the SRAM parameters such as small area, low power dissipation, high SNM. Following table shows the transistor sizing and transistor ratio of the CNFET 6T SRAM.

Table 6.7: Transistor sizing of the CNFET SRAM.

Transistor	Number of Tubes
Pull up Transistor	2
Pull down Transistor	10
Access Transistor	5

Table 6.8: Ratio sizing of the CNFET SRAM.

Cell Ratio	Pull up Ratio
2	0.4

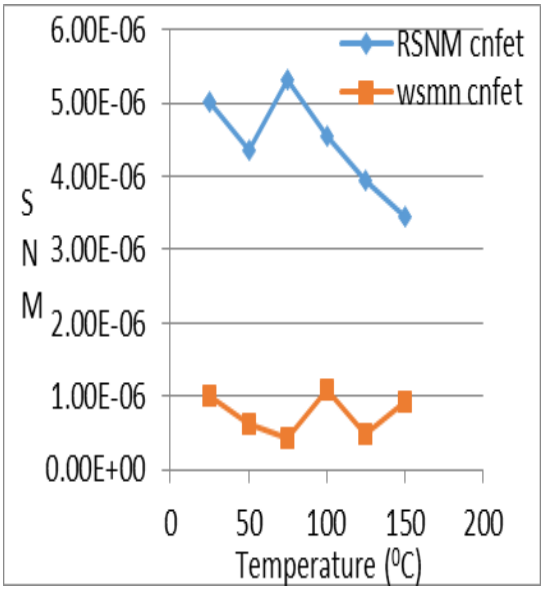


Figure 6.4: CNFET response by change in temperature.

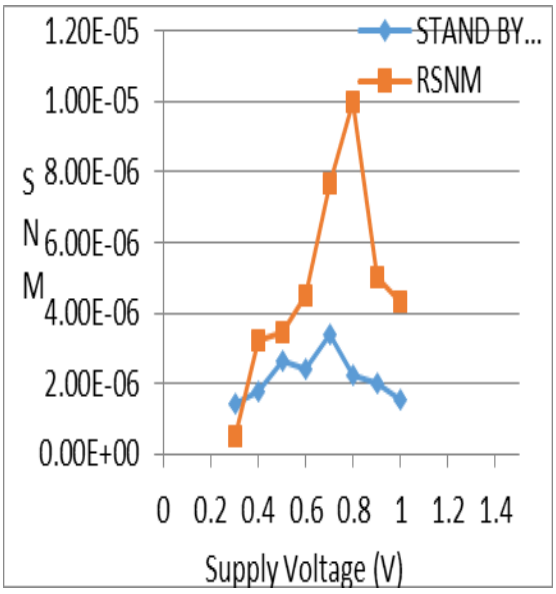


Figure 6.5: CNFET response by change in supply voltage.

Fig. 6.4 shows the various temperatures reading of the CNFET Transistor for design a 6T SRAM cell. Fig. 6.5 shows the various supply voltage reading of the CNFET Transistor for design a 6T SRAM cell.

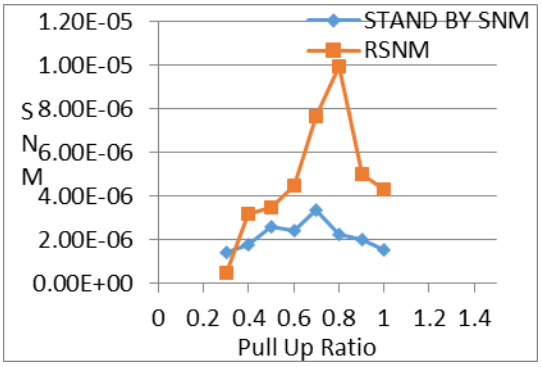


Figure 6.6: CNFET response by change in Pull Up ratio.

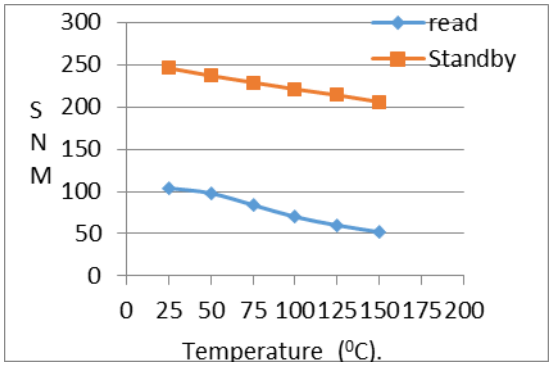


Figure 6.7: CMOS response by change in temperature.

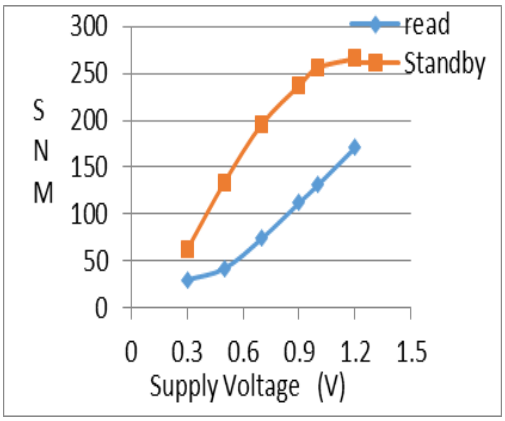


Figure 6.8: CMOS response by change in supply voltage.

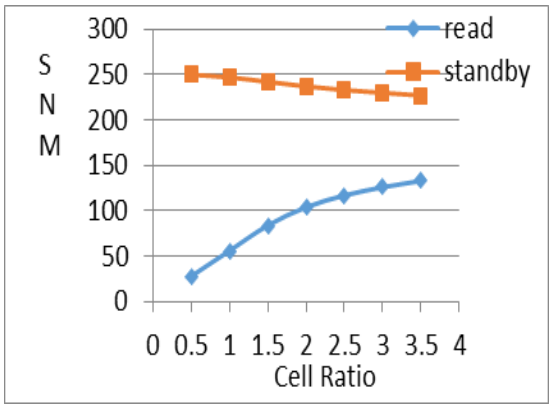


Figure 6.9: CMOS response by change in cell ratio.

Fig. 6.6 shows the various reading by change in WL of the CNFET Transistor for design a 6T SRAM cell. Fig. 6.7 shows the various reading by change in temperature of CMOS Transistor for design a 6T SRAM cell. Fig. 6.8 shows the various reading by change in supply voltage of CMOS Transistor for design a 6T SRAM cell. Fig. 6.9 shows the various reading by change in cell ratio CMOS Transistor for design a 6T SRAM cell.

6.1.2 Analysis of a Source Coupled VCO:

The 7 series FPGAs have complex and direct clocking arrangement with fixed global and locational I/O's which are managed by clocking resources. The CMTs (Clock Management Tiles) give clock for different applications viz. jitter filtering functionality and frequency synthesis. There are 24 CMTs wherein; each CMT has one PLL and one MMCM for PLL wherein the VCO is an important block. The ring oscillator with numerous stages indicates less oscillation frequency, so to defeat this trouble the source coupled voltage controlled oscillator (SCVCO) is outlined in this

work. The customary SC-VCO and AVLG based SC-VCO are sketched out using CMOS for upgrading the oscillation frequency. The execution of the proposed circuit is reproduced using Hspice programming hspice_a-2008.03 frame with the 32nm mode. The proposed AVLG based SC-VCO demonstrates higher faltering frequencies than the ordinary SC-VCO. Analysis of the input voltage, temperature and gate length variations on oscillation frequency and average power is carried out extensively.

The CMTs gives clock for different applications like jitter filtering functionality and frequency synthesis. Local routing is a non-clock asset which is not defined at the time of planning for clock functions. CMT has one PLL, and another one is MMCM, reside in the CMT column next to the I/O section. CMTs regularly find out global clock buffers to check out the clock distribution delay and change in the clock delay on another clock delay. Within CMTs MMCMs and PLLs work as frequency synthesizers, jitter channels, deskew tickers for a wide variety of frequencies, either outside or inside internal blocks respectively. Sometimes the PLL is a subset of MMCM functions. In the seven series FPGA, clock connectivity network allows different assets to provide the reference clocks to the MMCM and PLL. To gather clock system parameters GUI interface is used. The clocking wizard picks the suitable CMT asset and ideally arranges the CMT asset and related clock routing assets [124].

The MMCM and PLL offer numerous qualities. These two works as frequency synthesizers and jitter channel for a wide variety of frequencies and in-coming clock respectively. At the focal point of the two sections is a VCO, which accelerates and backs off dependent upon the voltage it gets from the PFD. The PFDs have three unique arrangements like D, M, and O. The pre-divider D (programmable by setup and a while later by methods for DRP) decreases the information repeat and supports one commitment of the regular PLL organize/repeat comparator. The feedback divider M (programmable by course of action methods for DRP) goes about as a multiplier since it isolates the VCO yield repeat before empowering the other commitment of the stage comparator. D and M must be picked genuinely to keep the VCO inside its predefined repeat run. The VCO has eight additionally scattered yield stages (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each can be driven one of the yield dividers (six for the PLL, O0 to O5, and seven for the MMCM, O0 to O6), each programmable by setup to section by any number from 1 to 128.

The MMCM and PLL have three data jitter channel decisions: low data transmission, high trade speed, or upgraded mode. The low-data trade restrict mode has the best jitter crippling yet not the most small stage counterbalance. The high-transmission limit mode has the best stage balance, yet not the best jitter reducing. The streamlined mode empowers the contraptions to find the best setting [125]. A VCO is a crucial building ruin in Phase Lock Loop (PLL), which picks the power bolstered by the PLL and range controlled by the PLL. There are two classifications of VCO like CS-VCO and SC-VCO [126].

I. Device Structure

This section herewith presents a source coupled VCO utilizing CMOS strategy. To fulfill the Barkhausen oscillation criteria, ring oscillator plots more than two delay segments. To improve the oscillation frequency, no of delay sections should be less. For one delay cell, it gives 180 phase shift hence, the wavering recurrence is enhanced and decreased the power utilization utilizing single stage VCO. The MOS transistor is a voltage controlled gadget which is utilized for current spill out of drain and source terminals with the control of entryway voltage. The PMOS has drain and source with p+ doping's and which are separated by distance L. The interfacing between two is called as a gate, and it is attached by silicon dioxide material whereas NMOS has N+ doping within lightly doped p substrate.

A singular stage SC-VCO circuit can be intended to scatter less power than ring oscillator. The circuit is drawn in Fig. 6.10. MOSFETs M0 and M1 are work as load, and they pull the output of SC-VCO. The MOSFETs M4 and M5 are used to sink a current I_d to perform as a constant-current source. MOSFETs M2 and M3 act as switches. The voltage at point out1 is larger than the voltage at point out2, as MOSFET M2 is off and M3 is on. Therefore, the capacitor is altered by I_d current due to M6 which is work as a constant current source and which sinks Id current and the flow of current through M3 is $2I_d$ [127]. The capacitor is fully charged when the voltage values of point X and Y are same. The value of I_d current through capacitor C will change the value of point X to discharge capacitor C down towards ground. The MOS M1gets ON M3 gets OFF when the point X goes to zero [128].

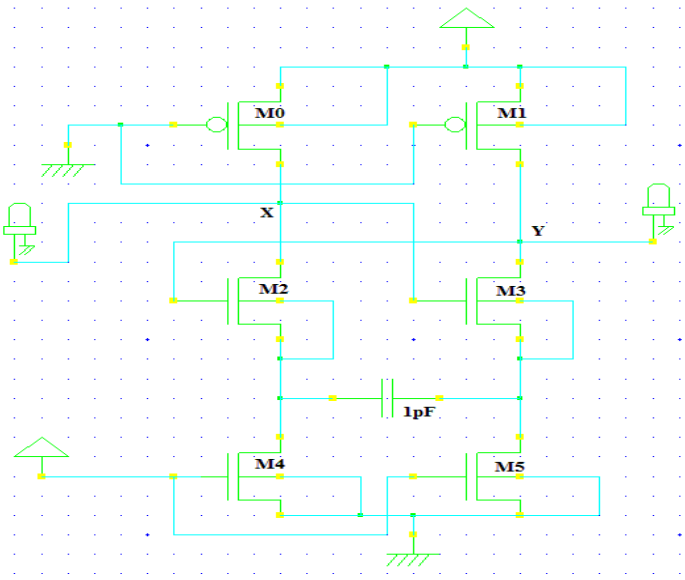


Figure 6.10: The structure of the single stage SC-VCO [129].

An AVL control circuit can be utilized in two ways, either at the upper end or the lower end of the cell to the cell to decrease supply voltage (AVLS plan) and to raise the capability of the ground node respectively. Fig. 6.11 demonstrates the circuit of a single stage SC-VCO with AVLG plan.

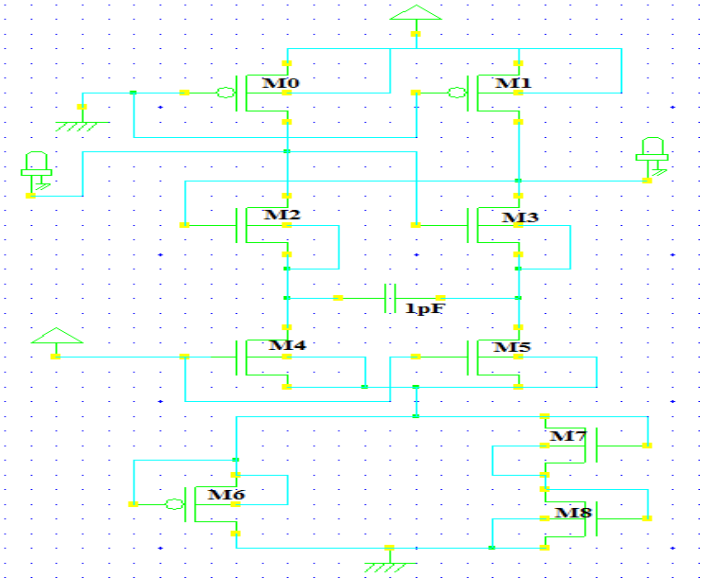


Figure 6.11: VCO using AVLG technique.

The used switch gives two different levels of voltage at the ground node and raised ground level during active and inactive mode respectively. This plan is like the diode footed supply plan proposed to control entryway and sub-edge spillages in single stage source coupled VCO, in which a diode made out of high Vt MOS transistor was used to raise the ground level of VCO in the idle mode [126].

The Centre drain current of VCO is identify by equation [127],

$$I_d centre = N * V_{DD} * C_{total} * F_{cen} \quad \text{.....(6.3)}$$

In the above condition V_{DD} =0.9V, 'C_{total}' is the aggregate capacitance of VCO and 'F_{cen}' is the middle oscillating frequency of VCO which rely upon the delay of the VCO [5]. The voltage esteem at point X is diverse before exchanging happens. To change the voltage level at point X, time required for switching is [128],

$$\Delta t = 2Vthn*C/I_d \quad \text{.....(6.5)}$$

This time take point X to change up to 2Vthn. As this circuit has the symmetrical structure, it means it has two stages. Therefore, discharge time is required for every cycle of the oscillator to find out oscillation frequency which is given as [126],

$$F_{osc} = \Delta t/2 = I_d*2*C*2V_{th} \quad \text{.....(6.6)}$$

Parameter evaluation has been done utilizing transient investigation. The condition for engendering delay is,

$$t_p = t_{pdr} + t_{pdf} \quad \text{.....(6.7)}$$

The equation for total delay is,

$$TPD = \frac{t_p}{2} \quad \text{.....(6.8)}$$

The power delay product is,

$$PDP = TPD * average\ power \quad \text{.....(6.9)}$$

The energy delay product is,

$$EDP = PDP * t_p = p_{avg} * t_p^2 = \frac{C_L*VDD^2*t_p}{2} \quad \text{.....(6.10)}$$

II. Simulation results

The simulation results of conventional SC-VCO and AVLG based SC-VCO with average power for input variations are listed in Table 6.10. Keeping V_{DD} =0.9V and C_L=1pF the temperature variations are listed in Table 6.11. By applying Vin = 0.7V, at V_{DD} =0.9V and CL=1pF the resulted gate length variations are listed in Table 6.12. The reaction to the swaying recurrence for input varieties are recorded in Table 6.13 for V_{DD} = 0.9V and CL=1pF. Temperature varieties are recorded in Table 6.14 for V_{DD} =0.9V, Vin = 0.7V, and CL=1pF. At long last, entryway length varieties are recorded in Table 6.15 when V_{DD} = 0.9V and Vin = 0.7V.

Table 6.9: Results of conventional SC- VCO and AVLG based SC-VCO with average power for input variations.

Input Voltage (V)	**Average power of AVLG based SC-VCO (µW)**	**Average power of SC-VCO (µW)**
0.85	0.614	0.764
0.80	0.603	0.756
0.75	0.586	0.744
0.70	0.561	0.735
0.65	0.519	0.716

Table 6.10: Results of conventional SC-VCO VCO and AVLG based SC-VCO with average power for temperature variations.

Temp (^{0}C)	**Average power of AVLG based SC-VCO (µW)**	**Average power of SC-VCO (µW)**
25	0.561	0.741
30	0.561	0.740
40	0.562	0.733
50	0.563	0.719
60	0.564	0.718
70	0.565	0.721
80	0.566	0.730
90	0.567	0.742
100	0.569	0.744

Table 6.11: Results of conventional SC-VCO and AVLG based SC-VCO with average power for gate length variations.

Gate length (L_{min})(µm)	**Average power of AVLG based SC-VCO (µW)**	**Average power of SC-VCO (µW)**
304	0.626	0.825
307	0.612	0.807
310	0.599	0.788
314	0.583	0.766
317	0.571	0.743
320	0.561	0.741
323	0.550	0.709
326	0.541	0.703
330	0.529	0.704
333	0.520	0.672
336	0.512	0.645

Table 6.12: Results of conventional SC-VCO and AVLG based SC-VCO with oscillation frequency for input variations.

Input Voltage (V)	**Oscillation frequency of AVLG based SC-VCO (MHz)**	**Oscillation frequency of SC-VCO (MHz)**
0.80	204	96.8
0.75	230	110
0.70	259	120
0.65	301	146
0.60	367	174
0.55	498	206

Table 6.13: Results of conventional SC-VCO and AVLG based SC-VCO with oscillation frequency for Temperature variations.

Temp (^{0}C)	**Oscillation frequency of AVLG based SC-VCO(MHz)**	**Oscillation frequency of SC VCO (MHz)**
25	565	146
30	552	143
40	488	136
50	439	131
60	420	121
70	366	120
80	342	115
90	339	112
100	320	103

Table 6.14: Results of conventional SC-VCO and AVLG based SC-VCO with oscillation frequency for Gate length variations.

Gate length (L_{min})(µm)	Oscillation frequency of AVLG based SC-VCO (MHz)	Oscillation frequency of SC-VCO (MHz)
307	1460	264
310	922	226
314	826	181
317	625	164
320	565	146
323	495	131
326	417	117
330	368	103
333	335	95.0
336	303	85.6

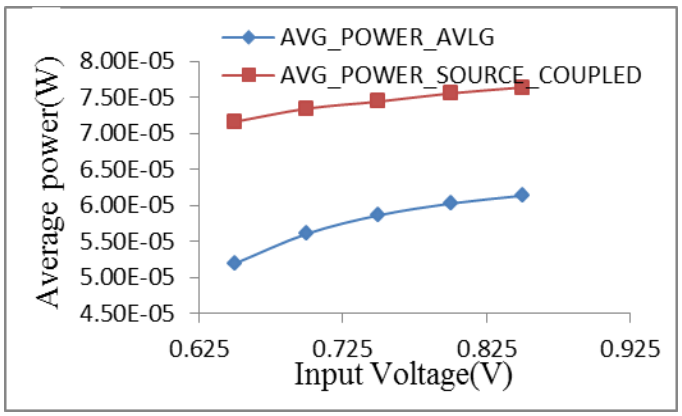


Figure 6.12: Average power V/s Input voltage readings of AVLG based SC-VCO and conventional SC-VCO.

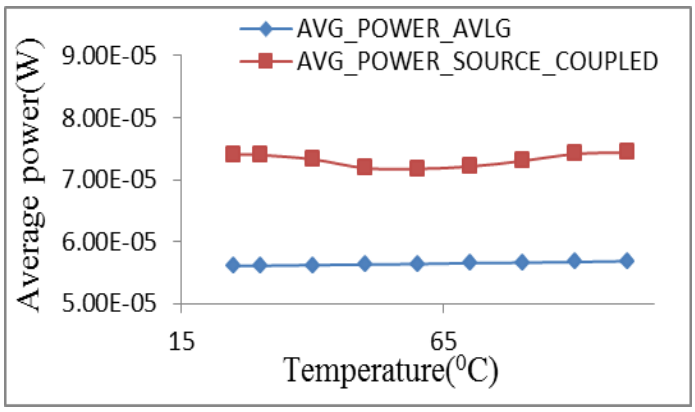


Figure 6.13: Average power V/s Temperature readings of AVLG based SC-VCO and conventional SC-VCO.

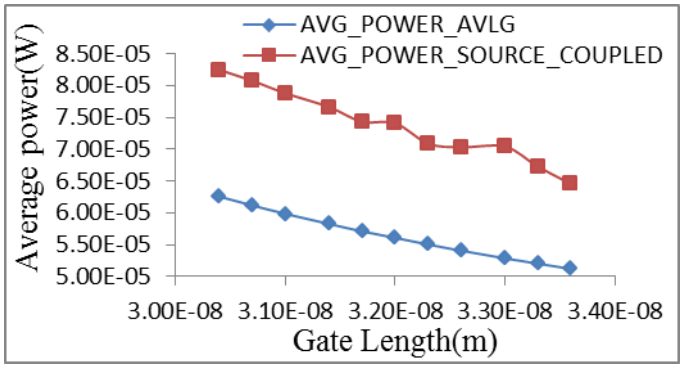


Figure 6.14: Average power V/s Gate length readings of AVLG based SC-VCO and conventional SC-VCO.

The graphical representations of conventional SC-VCO and AVLG based SC-VCO are drawing in Fig. 6.12 to 6.14. As input voltage and temperature increases its average power gets increased in both designs but AVLG based SC-VCO shows minimum average lower as compared to conventional SC-VCO. While the decrement in gate length it reduces average power with large extent in AVLG based SC-VCO.

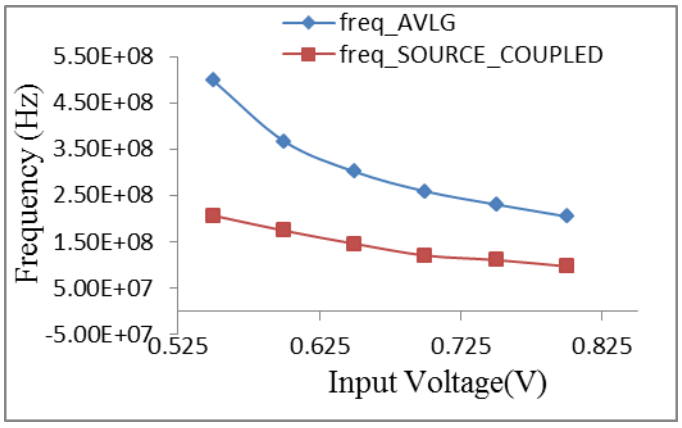


Figure 6.15: Oscillation frequency V/s Input voltage readings of AVLG based SC-VCO and conventional SC-VCO.

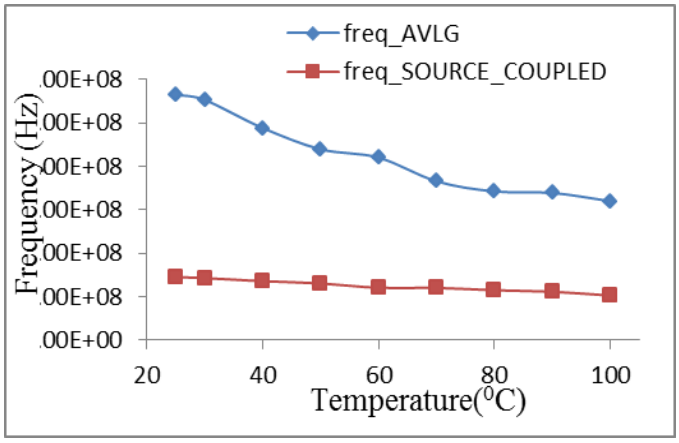


Figure 6.16: Oscillation frequency V/s Temperature readings of AVLG based SC-VCO and conventional SC-VCO.

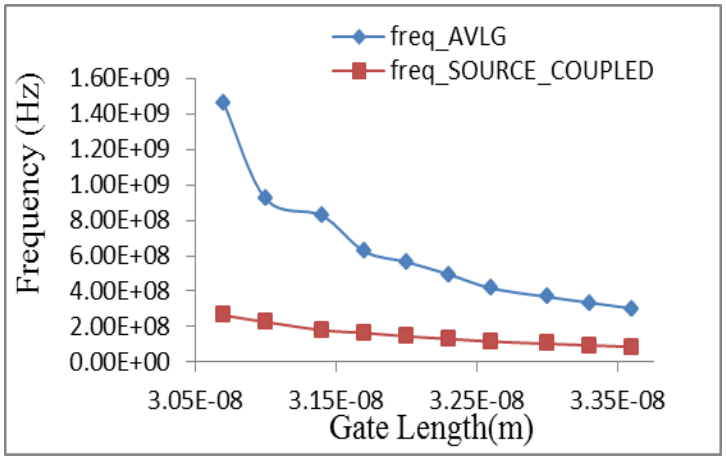


Figure 6.17: Oscillation frequency V/s Gate length readings of AVLG based SC-VCO and conventional SC-VCO.

The graphical representations of conventional SC-VCO and AVLG based SC-VCO are drawn in Fig.6.15 to 6.17. As input voltage, temperature and gate length increases its oscillation frequency get decreased in both designs, however, AVLG based SC-VCO shows maximum oscillation frequency range as compared to conventional SC-VCO.

The regular SC-VCO and AVLG based SC-VCO are outlined with CMOS 32nm innovation mode utilizing Hspice programming hspice_a-2008.03 variant. This work indicates higher recurrence range and lower normal power for AVLG based SC-VCO. AVLG design has a higher range of frequencies with the input voltage, temperature, and gate length variations. As input voltage changes from 0.80-0.55V, it has a 204-498MHz range of frequency. As temperature varies from 25-100^{0}C its frequency changes 565-320MHz. with gate length variations from 307-333µm its frequency range is 1460-303MHz. This range of maximum frequency can have used in clock circuitry of FPGA to reduce power dissipation of FPGA.

6.1.3 Analysis of Synchronous 4-Bit up Counter using SSASPL:

Low power, less delay and area efficient sequential circuit design has been the major concern for VLSI designers. The selection of optimized design technology plays a key role in achieving the above parameters. The standard cell library comprises of a few individual cells, which can fit for performing diverse logic usefulness. These standard cells are diverse in size and execution. Flip-flop is a vital part in each standard cell library. It is a result of its significance in the synchronous circuit outline. Flip-flops and latches are essential components in the plan of VLSI

circuits in digital design flip-flops and latches are basic storage elements. Flip flops are precarious timing elements in digital circuits which have a great impact on speed and power consumption. The Shift register is a sort of successive circuit it is predominantly utilized for capacity or exchange computerized information. An M-bit shift register consists of M -data flip-flops which are connected in series.

Low power consumption and area reduction is one of the main objectives in the designing of VLSI design. The Shift register is the essential building hinder in VLSI circuits. It is commonly used as a piece of various applications. The outline of shift register enlist is extremely clear. The M bit shift register enlist can be is made out of M data flip-flops. The littlest flip-flops are reasonable for outlining of move enlist to decrease the territory and power utilization. A latch can catch information amid the delicate time dictated by the width of clock waveform. In the event that the pulse clock waveform triggers a latch, the latch is synchronized with the clock also to edge-activated flip-flop in light of the fact that the rising and falling edges of the pulse clock are practically indistinguishable as far as timing. With this approach, the portrayal of the setup times of pulsed latch are communicated as for the rising edge of the pulse clock, and hold times are communicated as for the falling edge of the pulse clock. This implies the portrayal of timing models of pulsed latches is like that of the edge activated flip-flop.

The counter diminishes area and power utilization by supplanting flip-flops with pulsed locks. The planning issue between pulsed latches is comprehended utilizing various non-cover delayed pulsed clock motions rather than a solitary beat clock flag. Few the pulsed clock signals are utilized by gathering the latches to a few sub shifter enroll and utilizing extra impermanent storage latches [132]. A low power area reduced and speed improved serial type daisy chain memory register also known as shift Register is proposed by using modified dock generator circuit and SSASPL. This latch based counter consumes low area and low power than other latches. There is a modified complementary pass logic based 4 bit dock pulse generator with low power and low area is proposed that generates small dock pulses with small pulse width. These pulses are given to the conventional shift register that results high speed.

B. D. Yung [130] presented a low-power and range effective shift register utilizing pulsed latches. The zone and power utilization are diminished by supplanting Flip-Flops with pulsed latches. This technique takes care of the planning issue between pulsed latches using various non-cover postponed pulsed clock motions in-

stead of the traditional single pulsed clock signal. A Surekha et.al [131] investigated a move enroll utilizing SSASPL. The range and power utilization are decreased by supplanting flip-flops with pulsed latches. More devices utilizing SSASPL was created utilizing 65nm CMOS process. As the technology decrease power reduces [132] Manish kumar Soni et.al reviewed Sequential circuits largely contribute to the power dissipation and propagation delay in a digital system. Elio. Consoli et.al [133] conveyed the execution assessment of another class of pulsed latches is presented and tentatively surveyed in 65-nm CMOS. Its restrictive push pull pulsed latches topology depends on a push pull final organize driven by two split ways with a contingent pulse generator. Pulsed latches is additionally appeared to significantly enhance the vitality proficiency contrasted with the cutting edge.

Now days the latches based design rather than of flip flops are increased to achieve the area reduction. Counting is an essential function of digital circuits. an advanced counter comprises of a gathering of flip-flops that change state (set or reset) in a recommended grouping. The essential function of a counter is to deliver a predefined yield design arrangement. This part proposed 4 bit up counter using SSASPL latch. In digital design flip-flops and latches are essential storage components. Flip flops are problematic planning components in digital circuits which greatly affect speed and power utilization. In VLSI chip configuration lessening power has turned into a critical thought of an execution and zone. The Shift register is a type of successive circuit it is basically utilized for capacity or exchange digital data. M-bit move enlist comprises of M - information flip-flops which are associated in arrangement [134].

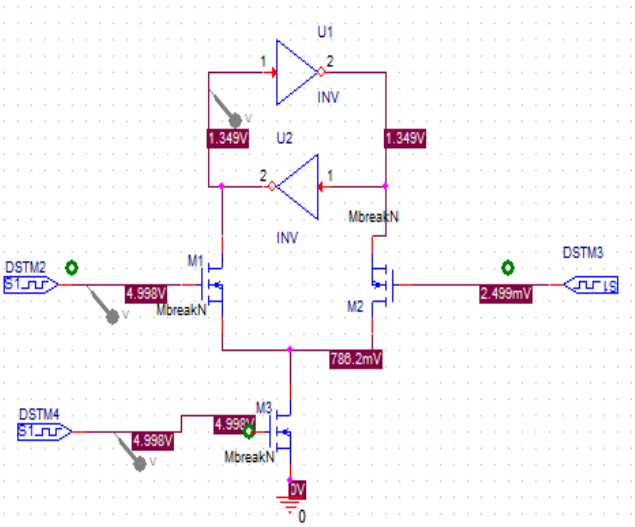


Figure 6.18: SSASPL using 7 transistors.

The SSASPL make utilization of the littlest scope of 7 transistors and it has a solitary transistor driven by utilizing the pulsed clock signal. The SSASPL invigorates the data with 3 NMOS transistors and it holds the data with 4 transistors in two cross-coupled invertors. It requires two differential data inputs and a pulsed clock signal [132]. Exactly when the pulsed clock signal is high, its data is revived. The draw down current of the NMOS transistors must be greater than the draw up current of the PMOS transistors in the invertors.

Both Latches and turn flops are circuit segments in which the yield is predicated upon the present commitments, and in addition depends on the past records and yields. The fundamental difference among the pulsed latch and flip flop is that a pulsed latch doesn't have a clock signal whereas the flip flop does possess it. There are different types of pulsed latch and flip flop. Contrasted with flip flops, pulsed latches have the benefits of requiring just a single lock arrange per clock cycle and of permitting time-obtaining crosswise over cycle limits. The flip-flops and pulsed latches where making plans issues are obtained which fathomed with the aid of such as postponed beat clock circuits in place of a solitary pulsed beat with the aid of gathering latches to a few sub move registers and additional stockpiling latch is used by the little pulsed clock signals. Here, use the Vdd is 2V and clock pulse is given in ms, the input signal is maximum 5V. Starting from 0s to 2ms the clock pulse is zero and input signal is 5v at 1ms to 2ms.

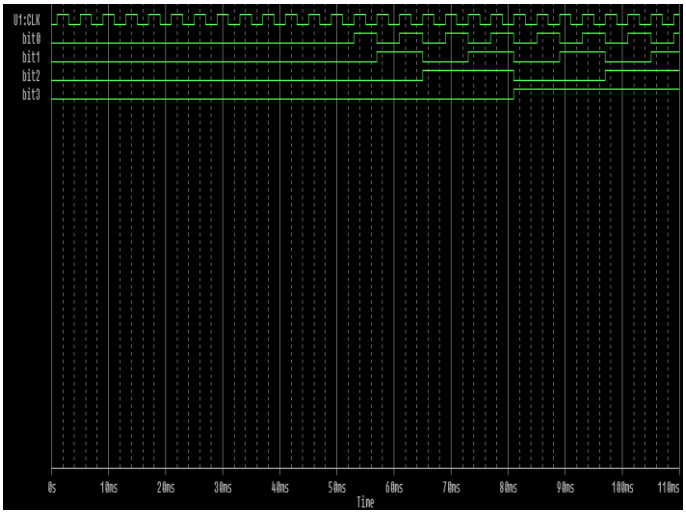


Figure 6.19: Simulation waveform for up counter using SSASPL.

Above Fig. 6.19 indicates the simulation end result for up counter the use of SSASPL. There's no inherent propagation put off in synchronous counter, due to the fact the whole counter levels are induced in parallel on the equal time, the maximum

running frequency of this form of frequency counter is much better than that for similar asynchronous counter circuits. Because this 4 bit synchronous counter counts sequentially on every clock pulse the ensuing outputs counts upward from 0(0000) to 15(1111).

Table 6.15: Obtained output sequence for Up counter.

Clock	**bit_3**	**bit_2**	**bit_1**	**bit_0**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Table 6.16: Transistor count and delay of the gates for various combinations [134].

Circuits	**Transistor count**	**Delay**
Inverter	2	11.04ns
NAND gate	4	20.92ns
AND gate	6	195.50ps
XOR gate	6	5.985ns
Master slave flip flop	42	11.22ns
Synchronous 4 bit up counter using M/s flip flop	210	20.39ns
Proposed 4 bit up counter using SSASPL	70	0.06ns

Above Table 6.16 shows that the transistor count of the gates, flip flop, latches used in existing and proposed design. Existing Johnson counter using master slave flip flop having 210 transistors. Our proposed Johnson counter using SSASPL having

70 transistors. Our proposed design shows 66.66% reduction in transistor count as compared to existing. There may be is no inherent propagation delay in synchronous counter, due to the fact entire counter levels are brought about in parallel on the equal time; the most operating frequency of this type of frequency counter is much better than that for similar asynchronous counter circuits.

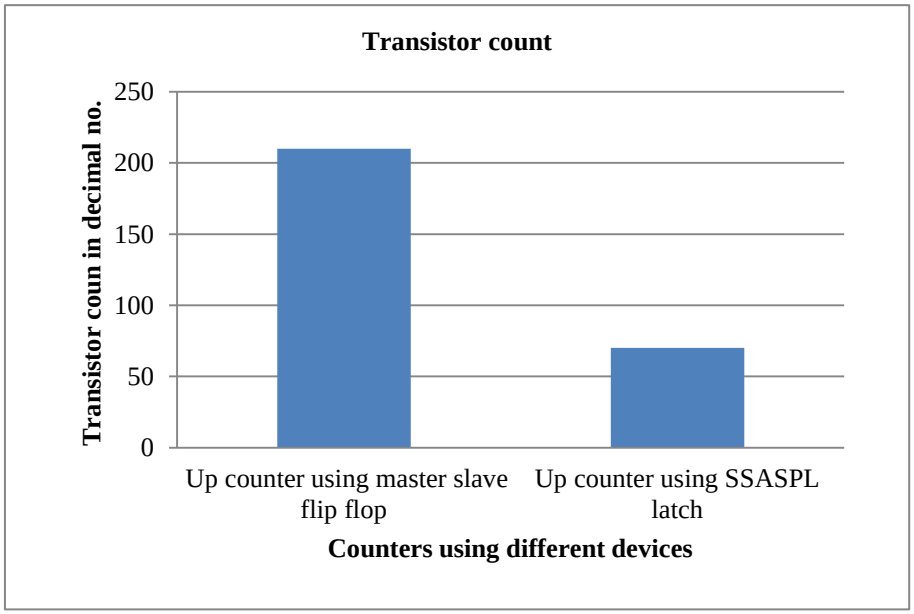


Figure 6.20: Graphical representation of Number of Transistors used for 4 bit up counter by using different devices.

Up counter design uses SSASPL latch which gives least transistor count. Design shows improvement because of SSASPL latch which having minimum number of transistors as compared to master slave flip flop. Proposed Up counter having 66.66% reduction transistor counts as compared to conventional Up-counter.

6.2 Summary

In CNFET inverter in explores an improvement in the results up to 79% than the conventional CMOS inverter. Here simulated the 6T SRAM in CNFET shows better performance. By comparing the readings of the 6T SRAM MOSFET and CNFET it has been observed that the read, write and hold maximum cell ration for read stability and minimum pull up ration for write operation is better for CNFET than MOSFET. As per the property of CNFET high supply voltage improves the high stability. The 6T SRAM CNFET having cell ration of 2 and pull up ratio of 0.4 improve and achieve maximum stability during read operation and also improve the standby mode operation compared with conventional CMOS SRAM.

The regular SC-VCO and AVLG based SC-VCO are outlined with CMOS 32nm innovation mode utilizing Hspice programming hspice_a-2008.03 variant. This work indicates higher recurrence range and lower normal power for AVLG based SC-VCO. AVLG design has a higher range of frequencies with the input voltage, temperature, and gate length variations. As input voltage changes from 0.80-0.55V, it has a 204-498MHz range of frequency. As temperature varies from 25-100^{0}C its frequency changes 565-320MHz. with gate length variations from 307-333µm its frequency range is 1460-303MHz. This range of maximum frequency can have used in clock circuitry of FPGA to reduce power dissipation of FPGA.

In this work the synchronous 4-bit up counter has been executed, simulated and analyzed. The execution of the counter is evaluated regarding transistor count and area. Design and execution of synchronous 4-bit up counter utilizing SSASPL is proposed which is upgrade in terms of area. Proposed Johnson counter using SSASPL having 70 transistors and 0.06ns delay. Design shows 66.66% reduction in transistor count as compared to existing. The proposed design is found to have good performance in terms of delay and transistor count.

Chapter 7

SUMMARY AND CONCLUSIONS

7.1 Introduction

FPGA are pre-fabricated silicon devices that can be configured to become almost any kind of digital circuits or systems. The “reconfigurable” term in FPGA indicates an ability to change its functionality even after fabrication. FPGAs are a popular choice for digital circuit implementation because of their growing density, speed, short design cycle, and steadily decreasing cost. However power consumption, especially leakage power, has become a major design hurdle for the semiconductor industry at the nanoscale regime. FPGA consumes significant amount of static as well as dynamic power due to the presence of additional logics for providing more flexibility as compared to an ASIC. Reconfigurability feature of FPGA is also attractive for the energy efficient devices. Though ASICs are more power efficient than FPGAs but they are expensive for lower volume and more difficult to design at a nanoscale.

Existing low power techniques are not sufficient to achieve the required ULP consumption and moderate speed in FPGA. Therefore, there is a pressing need to design ULP FPGA with reasonable speed so that they can replace ASICs used in ULP portable applications. Conventional devices designed for strong inversion region may not provide the optimum performance under subthreshold condition.

Hence, ULP consumption with moderate speed can be obtained by modifying existing low-power FPGA topologies or by optimizing the performance of Si-MOSFET device especially for Energy efficient applications. As further scaling of bulk MOS technology is very difficult due to increased static power and variability issues, there is need to design FPGA with devices beyond CMOS. Very few researchers have worked on designing field programmable gate arrays for portable applications.

This part is sorted out into four segments. The first section shows the outline of the work introduced in every section. The second section provides the conclusions drawn from the results obtained in each chapter. The third section summarizes the achievements and the last section outlines areas for future research.

7.2 Summary

ULP applications have extremely low power budget and moderate throughput requirement. Consequently power dissipation has developed as a key outline challenge for the scientists. The most optimum way to diminish the power consumption is by operating the transistor under super threshold conditions. However the circuits are extremely slow and prone to PVT variations. Hence, this thesis mainly targets area and moderate speed applications. It also explores the design of subthreshold FPGA so that the reconfigurability feature of the FPGA can be utilized in ULP applications. The summary of this is highlighted in this section.

Chapter 2 presented a brief overview of the technology scaling and sources of power dissipation. Power dissipation in CMOS circuits can be either unique or static (leakage). Not at all like dynamic power utilization, does the leakage current not rely upon the exchanging movement. It just relies upon the quantity of transistors on the chip. The dynamic power has overwhelmed control utilization in CMOS circuits; in any case, innovation scaling patterns have brought about leakage turning into a prevailing segment of aggregate power. The architecture of FPGA with its Structural and user programmable switch technologies are also briefly discussed. FPGA building blocks are also elaborated and the literature survey is reported.

Chapter 3 deals with the detailed literature review of the FPGA, the various CMOS and post CMOS devices up to the recent devices viz. TFET, FinFET and CNFET. Also a through survey about the Interconnects is also being covered which covers from the conventional Cu to the recent emerging interconnects viz. CNTs and GNRs. In chapter 4 executed the simulation work carried out on different devices of TFET. A comparison among the MOSFET and TFET is also reported for analyzing the difference of the performance parameters of the two.

In chapter 5 explored the interconnect simulations which are being carried out with different types of the interconnect materials like Cu, SWCNT, MWCNT, MCB, SLGNR and MLGNR. These simulations are even executed for different device types like MOSFET, TFET, FinFET and CNFET. The obtained results are compared for three different lengths viz. local, intermediate and global. It is proposed that there is a need of optimum utilization of the type of device and or interconnect for the interconnect length based on the performance parameters like PDP, PD and Pd.

Chapter 6 had dealt with the simulation work executed on the different digital domain circuits like SRAM cell, VCO and Pulsed latches. The performance parameters are explored and the same are also being reported about the enhancement of the results obtained in the individual type.

7.3 Conclusions

This thesis explored device, circuit and interconnect optimization techniques under subthreshold and super threshold conditions at different levels of the design hierarchy. The work presented in this thesis will enable to operate real time portable applications having moderate speed requirements under subthreshold conditions. This section highlights various conclusions drawn from the research work executed out in this thesis.

The low power techniques along with the FPGA architecture are well studied in chapter 2. The different schematics which play a pivotal role in the optimization of the IC are specified and the same are being reported. Also the FPGA family is explored for doing in-depth studies various families. Chapter 3 had explored a detailed survey about the devices and interconnects which are the major building blocks of the FPGA. Also along with it, the survey related to the digital circuits which are used in the digital domain is carried out.

Chapter 4 had reflected the simulation of the conventional MOSFET and the post-CMOS TFET. After analyzing the results it is concluded that the TFET based devices are having more advantages in terms of I_{ON}, I_{ON}/I_{OFF}, lesser leakage current, subthreshold swing lesser than 60 mV/decade etc.

Chapter 5 analyzed the performance of Cu, SWCNT, MWCNT, MCB and MLGNR interconnect incorporated with CMOS, CNFET, FinFET and TFET driver for local, intermediate and global level interconnect. PD and PDP is measured of each driver/interconnect combination. The interconnect capacitance impacts largely the delay at local level hence SWCNT performs better which has low capacitance value whereas interconnect resistance impacts delay largely at intermediate and global level hence MWCNT, MCB and MLGNR performs better which has low resistance values. Therefore, SWCNT is conceivable possibility for supplanting Cu at local level likewise MWCNT, MCB and MLGNR for intermediate and global level by utilizing CMOS, FinFET and TFET devices. However, utilizing CNFET driver MCB, MWCNT and MLGNR are appropriate for all level of interconnects compared to Cu interconnect technology.

In chapter 6 some of the basic digital schematics are being studied with their counterpart conventional circuits. The performance evaluation parameters reflect that there is an improvement in the performance of these schematics over its conventional counterparts.

7.4 Contributions

INTERNATIONAL JOURNAL

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Paper Status: **Under Review Process**.

7.5 Future Work

Increased static power dissipation and variability issues in bulk CMOS compels to investigate the suitability of beyond CMOS devices for FPGA. Hence, there is pressing need of improving the performance and energy efficiency of FPGAs using TFET or CNFET for portable applications. The TFET designs based on two source regions, dopingless TFET and vertical TFETs are few of the upcoming areas wherein the enhancement of the device characteristics, optimization of the device for best results can be predicted ahead with further refinements.

The emerging interconnects viz. CNTs, GNRs, OI are the best option in years ahead to come which encompasses with the lowered PD, PDP, EDP, increased speed etc. at different lengths of the interconnects. Interconnect viz. CNTs and GNRs have ample potentials to work in conjunction with conventional copper interconnect. Also the GNR based TFETs are also evolving to give a breakthrough over the areas of edge saturation.

The different internal schematics of FPGA viz. Memristor based schematic, refined 4T hybrid LUT, one level RRAM based mux etc. are some out of the broad areas wherein further research work can be executed.

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